



STIC Search Report

EIC 2800

STIC Database Tracking Number: 107864

TO: David Hogans
Location: CP4 4D14
Art Unit : 2813
Friday, November 14, 2003

Case Serial Number: 09/960495

From: Irina Speckhard
Location: EIC 2800
CP4-9C18
Phone: 308-6559

irina.speckhard@uspto.gov

Search Notes

Examiner Hogans,

Please find attached first-pass prior-art search results from the patent and non-patent abstract databases. The results were based on claims and statements of technical problems and solutions. Tagged records might be worth your review as well as the rest of the references provided.

If you need further searching or have questions or comments, please let me know.

Thank you,

Irina Speckhard

6780 107864

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-3429.

Date 11-06-03 Serial # 09/960,495 Priority Application Date 3-05-01
 Your Name David Hagan Examiner # 79069
 AU 2813 Phone 305-3361 Room CP4-4014
 In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

11-06-03 P04:33 IN

Where have you searched so far on this case?

Circle: USPT SWPI EP Abs JP Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements.

US 2002/0033519 to Babcock et al
5,589,708 to Kalnitsky → both in center backsee also JP 09-064279
to Kenji et al
also in center back

What types of references would you like? Please checkmark:

Primary Refs ☒ Nonpatent Literature ☒ Other _____
Secondary Refs _____ Foreign Patents ☒ _____
Teaching Refs _____What is the topic, such as the novelty, motivation, utility, or other specific facets defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Pls. Search Clms 1+4 Copies in center back

novelty: ^{clm1} resistor/passive device formed on a insulator w/
active regions on either side of insulator (inverted
transistor) see Fig 1b^{clm1}
predetermined width defn. by # of shift in resistance
i.e. - Resistance = (resistivity * length) / area
∴ if Resistance ↓ width ↑ and vice versa → a larger
width resistor will display less resistance

Staff Use Only

Searcher: Speckhard

Searcher Phone: _____

Searcher Location: STIC-EIC2800, CP4-9C18

Date Searcher Picked Up: 11/13/03Date Completed: 11/14/03Searcher Prep/Rev Time: 170Online Time: 70

Type of Search

Structure (#) _____

Bibliographic ☒

Litigation _____

Fulltext _____

Patent Family _____

Other _____

Vendors

STN ☒Dialog ☒

Questel/Orbit _____

Lexis-Nexis _____

WWW/Internet _____

Other _____

11/14/2003

09/960,495

14nov03 10:55:57 User267149 Session D1100.1

SYSTEM:OS - DIALOG OneSearch

File 2:INSPEC 1969-2003/Nov W1
(c) 2003 Institution of Electrical Engineers
*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 6:NTIS 1964-2003/Nov W3
(c) 2003 NTIS, Intl Cpyrght All Rights Res
File 8:Ei Compendex(R) 1970-2003/Nov W1
(c) 2003 Elsevier English Info. Inc.
File 34:SciSearch(R) Cited Ref Sci 1990-2003/Nov W2
(c) 2003 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info
File 35:Dissertation Abs Online 1861-2003/Oct
(c) 2003 ProQuest Info&Learning
File 65:Inside Conferences 1993-2003/Nov W2
(c) 2003 BLDSC all rts. reserv.
File 94:JICST-EPlus 1985-2003/Nov W2
(c)2003 Japan Science and Tech Corp(JST)
File 99:Wilson Appl. Sci & Tech Abs 1983-2003/Oct
(c) 2003 The HW Wilson Co.
File 144:Pascal 1973-2003/Nov W1
(c) 2003 INIST/CNRS
File 305:Analytical Abstracts 1980-2003/Oct W3
(c) 2003 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2003/Oct
(c) 2003 DECHEMA
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200373
(c) 2003 Thomson Derwent
File 347:JAPIO Oct 1976-2003/Jul(Updated 031105)
(c) 2003 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.
File 344:Chinese Patents Abs Aug 1985-2003/Apr
(c) 2003 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	64064	RESIST??????(3N) (PASSIV????? OR ELEMENT? ?)
S2	1913686	INSULAT??????? OR DIELECTR??????
S3	79026	ACTIV??????(3N) REGION? ?
S4	117252	(PREDETERMIN?????? OR PRE() DETERMIN????? OR SET OR DETERMI- N?????) (3N) (WIDTH OR WIDE??? OR LENGTH OR LONG???)
S5	77662	(SHIFT??? OR WIDTH OR WIDE??? OR DIMENSION? ? OR ELEMENT? - ?) (3N) RESIST??????
S6	353578	(ISOLAT???????? OR OXIDE) (3N) (LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI() LAYER????? OR SPACER??? OR INTERL- AYER????? OR INTER() LAYER????? OR MULTIPLE() LAYER? ?)
S7	59897	TRENCH? ? OR STI OR SHALLOW() TRENCH() ISOLATION
S8	405488	S6:S7
S9	23262	CMP OR CHEMICAL() MECHANICAL() POLISHING
S10	54930	POLISH??????(3N) (LAYER??? OR FILM??? OR COAT??? OR SURFACE? ?)
S11	86257	(DUMMY OR GATE???) (3N) ELECTRODE? ?
S12	748	CONCAV??????(3N) FORMAT??????
S13	73678	S9:S10
S14	9758	S1 AND S2
S15	61	S14 AND S3
S16	2	S15 AND S4
S17	59	S15 NOT S16
S18	59	S17 AND S5
S19	20	S18 AND S8
S20	2	S19 AND S13
S21	18	S19 NOT S20
S22	6	S21 AND S11
S23	6	RD (unique items)
S24	12	S21 NOT S22
S25	0	S24 AND S12
S26	12	RD S24 (unique items)
S27	134	S1 AND S13
S28	132	S27 NOT S19
S29	18	S28 AND S8
S30	13	S29 AND S5
S31	13	RD (unique items)
S32	5	S29 NOT S30
S33	5	RD (unique items)
S34	13	S31 NOT S32
S35	3	S34 AND S3
S36	10	S34 NOT S35
S37	5	S36 AND S2
S38	5	S36 NOT S37
S39	5	RD (unique items)
S40	6909	S8 AND S13
S41	23	S40 AND S5
S42	8	S41 NOT S19, S29
S43	8	RD (unique items)

11/14/2003

09/960,495

16/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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007705801

WPI Acc No: 1988-339733/198848

XRAM Acc No: C88-150122

XRPX Acc No: N88-257598

Semiconductor laser device capable of high speed modulation - utilising
active region with relatively smaller forbidden band width
than surrounding semiconductor layer

Patent Assignee: TOSHIBA KK (TOKE)

Inventor: FURUYAMA H; HIRAYAMA Y; MORINAGA M; NAKAMURA M; OKUDA H; SUZUKI N

Number of Countries: 005 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 293185	A	19881130	EP 88304737	A	19880525	198848 B
JP 63292687	A	19881129	JP 8726944	A	19870526	198903
JP 1048483	A	19890222	JP 87204223	A	19870819	198914
JP 1084686	A	19890329	JP 87240845	A	19870928	198919
US 4862474	A	19890829	US 88198866	A	19880526	198944
US 4974232	A	19901127	US 89383099	A	19890721	199050
EP 293185	B1	19940202	EP 88304737	A	19880525	199405
DE 3887567	G	19940317	DE 3887567	A	19880525	199412
			EP 88304737	A	19880525	

Priority Applications (No Type Date): JP 87240845 A 19870928; JP 87126944 A
19870526; JP 87204223 A 19870819; JP 8726944 A 19870526

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 293185	A	E			
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Designated States (Regional): DE FR GB

US 4862474	A		30		
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EP 293185	B1	E	38	H01S-003/19	
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Designated States (Regional): DE FR GB

DE 3887567	G			H01S-003/19	Based on patent EP 293185
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Abstract (Basic): EP 293185 A

A semiconductor laser device comprises a substrate (10) having a first semiconductor layer (11) of a first conductivity type; and a semiconductor laser element (50) provided on substrate, which includes a mesa portion (20) having a second semiconductor layer (13) provided above (11) and of a second conductivity type; an **active region** (12a) consisting of a semiconductor formed between (11) and (13), which contributes to light emission; electric **insulating** regions are formed on opposite sides of buried portion and between (11) and (13); first and second electrodes (16,17) for supplying current to (12a). The (50) includes a pair of buried portions (13a) consisting of a semiconductor formed on and contiguous to opposite sides of width of **active region** (12a), and having a greater forbidden band width than the energy gap of **active**

*****region*****. An auxiliary mechanism (51) is provided on substrate and side by side with semiconductor laser element, and includes a third semiconductor layer (13B) of same material as buried portions; a high resistivity layer on (13B) and on electrode take out pad portion provided on high resistivity layer and electrically connected to first electrode of semiconductor laser *****element*****. Pref. the high

resistivity layer is integrally connected to at least one side of laser element to provide mechanical support, and includes an auxiliary mesa portion (20a) having an electric **insulating** region formed between high resistivity layer and semiconductor layer.

USE/ADVANTAGE - High performance semiconductor laser device with reduced contact resistance, exhibits high speed modulation and is satisfactorily combined with a passive element or auxiliary element. The device has improved mechanical strength, yield, reliability and cost

Abstract (Equivalent): EP 293185 B

A semiconductor laser device comprises a substrate (10) having a first semiconductor layer (11) of a first conductivity type; and a semiconductor laser element (50) provided on substrate, which includes a mesa portion (20) having a second semiconductor layer (13) provided above (11) and of a second conductivity type; an **active region** (12a) consisting of a semiconductor formed between (11) and (13), which contributes to light emission; electric **insulating** regions are formed on opposite sides of buried portion and between (11) and (13); first and second electrodes (16,17) for supplying current to (12a). The (50) includes a pair of buried portions (13a) consisting of a semiconductor formed on and contiguous to opposite sides of width of **active region** (12a), and having a greater forbidden band width than the energy gap of **active**

*****region*****. An auxiliary mechanism (51) is provided on substrate and side by side with semiconductor laser element, and includes a third semiconductor layer (13B) of same material as buried portions; a high resistivity layer on (13B) and on electrode take out pad portion provided on high resistivity layer and electrically connected to first electrode of semiconductor laser *****element*****. Pref. the high **resistivity** layer is integrally connected to at least one side of laser element to provide mechanical support, and includes an auxiliary mesa portion (20a) having an electric **insulating** region formed between high resistivity layer and semiconductor layer.

USE/ADVANTAGE - High performance semiconductor laser device with reduced contact resistance, exhibits high speed modulation and is satisfactorily combined with a passive element or auxiliary element. The device has improved mechanical strength, yield, reliability and cost

Abstract (Equivalent): US 4974232 A

The device comprises (a) a substrate with a layer of 1st conductivity semiconductor and (b) a semiconductor laser element including (i) a mesa portion having a 2nd semiconductor layer of 2nd conductivity type, (ii) an **active region** including a semiconductor formed between the 1st and 2nd layers, having a **predetermined width** and an energy gap smaller than that of the 1st and 2nd layers, (iii) oscillating means to emit a laser beam from the **active region**, comprising a diffraction grating on the **active region**, (iv) a pair of buried portions formed on and contiguous to opposite sides of the act

US 4862474 A

Semiconductor laser device comprises; (a) a substrate with a first layer of a first conductivity type and (b) a semiconductor laser element and auxiliary mechanism side-by-side on he substrate. The laser element has a mesa portion with a semiconductor layer of a second conductivity type above the first layer.

It also has an **active region** of semiconductor between the first and second layers. This is of *****predetermined***** *****width***** and has an energy gap smaller than that of the first and second layers.

Its surfaces serve as reflecting mirrors and oscillate a laser beam between them and emit a beam from one of them, contributing to high emission.

A pair of buried semiconductivity regions is formed on opposite sides of the *****active***** *****region***** widthwise and touching them. These regions have a greater forbidden band width than the energy gap of the *****active***** *****region*****.

Insulating regions are formed on opposite sides of the buried regions and between the first and second semiconducting layers and first and second electrodes supply current to the **active** *****region*****. The auxiliary mechanism includes a third semiconductor layer made of the same material as the buried regions; a high resistivity layer is provided on top of this third layer; and on top of the high resistivity layer is an electrode take-out pad connected to the first electrode.

ADVANTAGE - *****Active***** *****region***** width can be controlled. Contact resistance can be reduced and high speed modulation is permitted.

16/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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03238685
MANUFACTURE OF SEMICONDUCTOR LASER

PUB. NO.: 02-214185 [JP 2214185 A]
PUBLISHED: August 27, 1990 (19900827)
INVENTOR(s): MIHASHI YUTAKA
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-035432 [JP 8935432]
FILED: February 15, 1989 (19890215)
JOURNAL: Section: E, Section No. 1000, Vol. 14, No. 515, Pg. 19, November 13, 1990 (19901113)

ABSTRACT

PURPOSE: To obtain a semiconductor laser with a low threshold value with improved reproduction and yield by performing ion implantation of first conductive and second conductive impurities ions from aslant upper direction of opposite direction for the mask length of mask for stripe-shaped implanted ion elements to form doped regions.

CONSTITUTION: A p-type or high-resistance clad layer 2, a quantum well active layer 3, an n-type or high-resistance clad layer 4, and a GaAs contact layer 5 are subjected to epitaxial growth in sequence on a semi-insulation GaAs substrate 1 and a stripe-shaped mask 6 for implantation ion *****elements***** consisting of photo *****resist***** is formed. Then, a p-type and n-type impurities atom ion is ion-implanted from aslant upper direction of opposite direction for the mask 6 for implantation ion elements and then p-type and n-type doped regions 8 and 7 are formed. Thus, it becomes possible to **determine** the **width** of an **active** *****region***** 9 in self-aligned manner without mask matching. Therefore, it is possible to obtain a horizontal semiconductor layer of low-threshold value oscillation with improved reproduction properties and yield.

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20/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014910805

WPI Acc No: 2002-731511/200279

XRPX Acc No: N02-576672

Semiconductor device for analog circuit, has **resistor elements** formed on **insulating oxide film** and **active regions** in contiguous with **resistor element**

Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ); MITSUBISHI DENKI KK (MITQ)

Inventor: AMISHIRO H; IGARASHI M; KUMAMOTO T; YAMAGUCHI K

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020123202	A1	20020905	US 2001960495	A	20010924	200279 B
JP 2002261244	A	20020913	JP 200159948	A	20010305	200279

Priority Applications (No Type Date): JP 200159948 A 20010305

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020123202	A1	19		H01L-021/20	
JP 2002261244	A	13		H01L-027/04	

Abstract (Basic): US 20020123202 A1

Abstract (Basic):

NOVELTY - Several **resistor elements** (4) are formed using a MOS transistor gate layer on an **insulating ***oxide*** ***film*****. Several *****active*** ***regions***** (3)

are

formed in contiguous with each **resistor element** cross-wire on both sides. The width of the *****oxide*** ***film***** is defined by an amount of **shift in resistance** value of the **resistor ***elements*****.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for semiconductor device manufacturing method.

USE - Semiconductor device for analog circuit.

ADVANTAGE - Allows the **oxide film** to be divided into suitable strips, forestalling a concave formation at the center of the **film** upon **polishing** of the **film** by **CMP**, thereby enhancing dimensional accuracy of the **resistor elements** upon fabrication. By presetting width of the *****oxide*** ***film*****, it is possible for the **resistor elements** to constitute semiconductor devices whose reliability is high enough to meet high precision requirements.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of the semiconductor device.

Active regions (3)

Resistor elements (4)

pp; 19 DwgNo 1A/14

20/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009777415

WPI Acc No: 1994-057267/199407

XRAM Acc No: C94-025762

XRPX Acc No: N94-045063

Mfr. of semiconductor device with buried elements in SOI substrate - by wafer bonding after forming electrical elements, saves chip area and is used for memory devices, transistors and resistors

Patent Assignee: ZH KANKOKU DENSHI TSUSHIN KENKYUSHO (KANK-N); KOREA ELEC & TELECOM RES INST (KOEL-N); KOREA ELECTRONICS & TELECOM RES (KOEL-N)

Inventor: KANG S; YOO H; KANG W; YU H

Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5286670	A	19940215	US 92880892	A	19920508	199407 B
KR 9306732	B	19930723	KR 917454	A	19910508	199407
JP 6061339	A	19940304	JP 92116093	A	19920508	199414

Priority Applications (No Type Date): KR 917454 A 19910508

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5286670	A	10		H01L-021/302	
JP 6061339	A	8		H01L-021/76	
KR 9306732	B			H01L-027/04	

Abstract (Basic): US 5286670 A

A wafer bonding method of mfg. a semiconductor device having buried electrical elements in a SOI substrate comprises forming an **isolating insulator layer** (27) at a seed wafer using an isolating mask, depositing a second **insulator** layer (29) over the first and the seed wafer and using a contact mask to define contact holes to form contacts on the seed wafer. A poly-Si layer is deposited on the second layer and contacts, doped and patterned to define an electrical element (31), around which an **insulating** layer (35) is deposited. A second poly-Si layer (33) is formed, doped for connecting to a handling wafer and *****polished***** to a mirror *****surface*****.

An **insulation** layer for connection is deposited on the handling wafer and thermally bonded to the mirror surface, and the seed wafer is polished until the first **isolating insulator** **polish stop layer** is exposed to give the SOI substrate with device *****active***** *****region*****.

USE/ADVANTAGE - SOI substrate with buried electrical elements for memory cells, transistors, *****resistors*****, etc. The electrical **element** is formed before wafer bonding and there is efficient use of the chip area.

Dwg.3D/3

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23/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014775521

WPI Acc No: 2002-596227/200264

XRAM Acc No: C02-168522

Method for fabricating high resistance device in semiconductor device
having salicide layer

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)

Inventor: KIM G J; YOON J M

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
KR 2002017365	A	20020307	KR 200050647	A	20000830	200264 B

Priority Applications (No Type Date): KR 200050647 A 20000830

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
KR 2002017365	A	1	H01L-021/336	

Abstract (Basic): KR 2002017365 A

Abstract (Basic):

NOVELTY - A method for fabricating a high resistance device in a semiconductor device having a salicide layer is provided to form a high resistance device in a semiconductor device having a salicide layer without an additional process.

DETAILED DESCRIPTION - A **gate electrode** and a conductive layer(24) are patterned on a substrate(20). A multitude of MOS transistor is formed on a region A1. A multitude of high *****resistance***** *****element***** is formed on a region A2. A **gate oxide layer** is inserted between the substrate(20) and the *****gate***** *****electrode*****. A size of the high *****resistance***** **elements** is smaller than a size of an active layer(22) forming a source/drain of the MOS transistor. A source/drain *****region***** and the **active layer(22)** are formed by using the **gate electrode** and the conductive layer(24) as an ion implantation mask. A source/drain region is formed on the region A1. An *****insulating***** material layer(26) is formed on the region A2. A metal layer is formed on a whole surface of the above structure. The metal layer is changed to a salicide layer(28a) by performing a rapid thermal silicidation process.

pp; 1 DwgNo 1/10

23/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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008859275

WPI Acc No: 1991-363299/199150

Related WPI Acc No: 1994-233908; 1998-494891; 1998-567678; 1998-570794;
1998-609419; 1999-582972

XRAM Acc No: C91-156511

XRPX Acc No: N91-278291

Formation of FET e.g. P-channel transistor used in CMOS SRAM - includes
mfr. of polycrystalline silicon channel over *****active***** *****region*****

EIC2800

Irina Speckhard

308-6559

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which acts as control gate for FET

Patent Assignee: STMICROELECTRONICS INC (SGSA); SGS-THOMSON MICROELTRN
INC (SGSA); SGS THOMSON MICROELTRN INC (SGSA)

Inventor: CHAN T C; GURITZ E H; HAN Y P; HAN Y; BISHOP W A

Number of Countries: 007 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 460833	A	19911211	EP 91304676	A	19910523	199150 B
US 5135888	A	19920804	US 89298530	A	19890118	199234
			US 90531014	A	19900531	
US 5196233	A	19930323	US 89298530	A	19890118	199314
JP 6342892	A	19941213	JP 91228110	A	19910531	199509
US 5770892	A	19980623	US 89298530	A	19890118	199832
			US 90531014	A	19900531	
			US 91798615	A	19911126	
			US 94218700	A	19940328	
			US 95460494	A	19950602	
EP 460833	B1	20000830	EP 91304676	A	19910523	200042
			EP 98201854	A	19910523	
			EP 99201796	A	19910523	
DE 69132387	E	20001005	DE 632387	A	19910523	200057
			EP 91304676	A	19910523	
KR 232505	B1	19991201	KR 918894	A	19910530	200111

Priority Applications (No Type Date): US 90531014 A 19900531; US 89298530 A
19890118; US 91798615 A 19911126; US 94218700 A 19940328; US 95460494 A
19950602

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 460833	A		8		
Designated States (Regional): DE FR GB IT					
US 5135888	A	7		H01L-021/44	CIP of application US 89298530
US 5196233	A	8		H01L-021/44	
JP 6342892	A	6		H01L-027/11	
US 5770892	A			H01L-027/11	CIP of application US 89298530 Div ex application US 90531014 Cont of application US 91798615 Cont of application US 94218700 Div ex patent US 5135888 CIP of patent US 5196233
EP 460833	B1 E			H01L-027/11	Related to application EP 98201854 Related to application EP 99201796 Related to patent EP 877425 Related to patent EP 952614
Designated States (Regional): DE FR GB IT					
DE 69132387	E			H01L-027/11	Based on patent EP 460833
KR 232505	B1			H01L-027/04	

Abstract (Basic): EP 460833 A

A method of fabricating an FET in an I.C. comprises the sequential formation of: and **active region** (16,18) in a Si substrate (10), a gate *****dielectric***** layer (22) and a polysilicon region (20). Source /drain regions are then formed in the poly Si so that a channel region is defined in the poly Si over the **active region**, wherein the **active region** acts as a control gate for the channel.

USE/ADVANTAGE - Useful as a load device for an SRAM cell (claimed). The device uses the same chip area as a resistive load cell.

In a CMOS SRAM the p-channel device provides high resistance when off and relatively low resistance when on compared with prior art. It is therefore more stable to noise and soft errors. The cell is faster due to higher switching current and works well with lower supply voltage.

Dwg.4/6

JP 6342892 A

A method of fabricating an FET in an I.C. comprises the sequential formation of: and **active region** (16,18) in a Si substrate (10), a gate *****dielectric***** layer (22) and a polysilicon region (20). Source /drain regions are then formed in the poly Si so that a channel region is defined in the poly Si over the **active region**, wherein the **active region** acts as a control gate for the channel.

USE/ADVANTAGE - Useful as a load device for an SRAM cell (claimed). The device uses the same chip area as a resistive load cell. In a CMOS SRAM the p-channel device provides high resistance when off and relatively low resistance when on compared with prior art. It is therefore more stable to noise and soft errors. The cell is faster due to higher switching current and works well with lower supply voltage.
(8pp Dwg.No.4/6

Abstract (Equivalent): US 5196233 A

Mfr. of semiconductor circuits comprises (a) forming a 1st layer of polycrystalline Si signal lines over the IC, (b) forming an **insulating** layer over the IC, (c) forming contact openings in the **insulating** layer to expose parts of the signal lines and substrate, (d) forming a 2nd polycrystalline-Si layer of 1st conductivity type, (e) forming 2nd-type regions in the 2nd polycrystalline-Si layer, and (f) patterning the 2nd polycrystalline-Si to form elongate elements having a 1st-type region between two separate 2nd-type regions. Current flowing through the element passes through the 2nd, 1st and 2nd type regions. The elongate elements made electrical contact with both the substrate and the exposed 1st polycrystalline-Si layer in the openings, thus forming a shared contact.

USE/ADVANTAGE - Used to mfr. a *****resistive***** load *****element***** for a semiconductor IC, esp. an SRAM, by a low temp. process which can be incorporated into any standard semiconductor fabrication process flow.

Dwg.3/6

US 5135888 A

Method comprises (a) forming an n-channel field effect device having source/drain regions opposite a **gate electrode** and a channel under the **gate electrode** within the substrates, (b) forming a gate **oxide layer** over the substrate, (c) forming an opening through the gate **oxide layer** to expose an underlying conductive region, (d) forming poly-Si over the gate **oxide layer** and conductive region, (e) forming p-type source/drain regions in the poly-Si, (f) forming a p-channel region in the poly-Si between the source/drain regions, and (g) etching the poly-Si to define an elongate p-channel element connecting the p-type source-drain regions.

The produced element is much longer than its width. Opt. a second n-channel transistor is formed where the exposed conductive region is it's source/drain region.

USE/ADVANTAGE - Used to mfr. a load element for a CMOS SRAM cell, which utilises p-channel transistors, using the same amt. of chip area as resistive load cells.

Dwg.4/5

11/14/2003

09/960,495

23/3,AB/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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07703759

SEMICONDUCTOR ELEMENT AND METHOD OF FORMING IT

PUB. NO.: 2003-197639 [JP 2003197639 A]
PUBLISHED: July 11, 2003 (20030711)
INVENTOR(s): KIM NAM-SIK
APPLICANT(s): HYNIX SEMICONDUCTOR INC
APPL. NO.: 2002-279822 [JP 2002279822]
FILED: September 25, 2002 (20020925)
PRIORITY: 01 200177847 [KR 200177847], KR (Korea) Republic of, December
10, 2001 (20011210)

ABSTRACT

PROBLEM TO BE SOLVED: To improve the operation characteristic of a semiconductor **element** by minimizing the **resistance** of an impurity junction region.

SOLUTION: This semiconductor element is provided with an SOI wafer with a laminated structure comprising a first silicon layer 11, a buried **insulation** film 13 and a second silicon layer 15, a **trench** 50 that is formed with the element isolation region of the second silicon layer removed, a first silicide layer 21 that is formed on the side wall of the **trench**, an element **isolation film** 23 defining an **active region** with the **trench** formed, a **gate electrode** 27 that is formed on the **active region** with the gate **insulator** film interposed, **insulator** film spacers 31 that are formed on both sidewalls of the **gate electrode**, impurity junction regions 29 and 33 that are formed in the **active region** on both sides of the **gate electrode** and a second silicide layers 35 that are formed on the top of the **gate electrode** and the impurity junction region.

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23/3,AB/4 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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05758407

SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 10-041507 [JP 10041507 A]
PUBLISHED: February 13, 1998 (19980213)
INVENTOR(s): ADACHI TETSUO
KATO MASATAKA
SUDO ITSUKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 08-197293 [JP 96197293]
FILED: July 26, 1996 (19960726)

ABSTRACT

PROBLEM TO BE SOLVED: To ensure the withstand voltage of a diffusion layer, and to prevent the fluctuation of MOS transistor characteristics and the lowering of **element isolation resistivity** by forming a structure in which a **gate electrode** and an **element isolation region**, and a **diffusion layer** and the **element isolation region** do not come into contact with each other.

SOLUTION: A **gate oxide film 2**, a polysilicon film 3 and Si(sub 3)N(sub 4) **insulating film 14** are coated on a P-type semiconductor substrate 1 by conducting a sacrificial **oxide film** formation and removing process, the polysilicon film and the Si(sub 3)N(sub 4) **insulating film** are processed on the part which becomes an **active region** by photoetching, and an Si(sub 3)N(sub 4) film 15 is formed on the whole surface. Anisotropic dry etching is conducted in such a manner that the Si(sub 3)N(sub 4) **insulating film 15** is left on the side face only of the polysilicon film 3 and the Si(sub 3)N(sub 4) film 14, a channel stopper layer 4 and an **element isolation layer 5** are formed, and the Si(sub 3)N(sub 4) film on the polysilicon 3 and the Si(sub 3)N(sub 4) film 15 on the side wall are removed. Accordingly, by providing a side wall consisting of a CVD **insulating film**, the threshold value of the MOS transistor in a microscopic region can be stabilized, and the lowering of the withstand voltage of the diffusion *****layer***** on an **element ***isolation***** end part can be prevented.

23/3,AB/5 (Item 3 from file: 347)
 DIALOG(R)File 347:JAPIO
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03564160

MIS TYPE SEMICONDUCTOR DEVICE

PUB. NO.: 03-227060 [JP 3227060 A]
 PUBLISHED: October 08, 1991 (19911008)
 INVENTOR(s): AEBA NOBUAKI
 APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
 (Japan)
 APPL. NO.: 02-022641 [JP 9022641]
 FILED: January 31, 1990 (19900131)
 JOURNAL: Section: E, Section No. 1151, Vol. 16, No. 4, Pg. 49, January
 08, 1992 (19920108)

ABSTRACT

PURPOSE: To improve a MIS type semiconductor in degree of integration without deteriorating a transistor in performance by a method wherein recesses or protrusions are provided to the surface of an **active region** on the primary face of a semiconductor substrate demarcated by an **element isolation insulating film**, and a MIS transistor is formed there.

CONSTITUTION: A reverse conductivity type island region 5 is formed, an **element isolation insulating film 3** is formed to demarcate an **active region 2**, a **resist** covering the **element isolation insulating film 3** is patterned, and an isotropic etching takes place using the patterned resist to form a groove. An silicon *****oxide*** ***film*** 6** is formed along the groove concerned, an **gate electrode 1** is formed, and a source and a drain are formed through an ion implantation method, whereby a basic cell composed of a P-channel MIS transistor and an N-channel MIS transistor is

formed.

23/3,AB/6 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
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01651636
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 60-130136 [JP 60130136 A]
PUBLISHED: July 11, 1985 (19850711)
INVENTOR(s): KOMATSU MICHIO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 58-237406 [JP 83237406]
FILED: December 16, 1983 (19831216)
JOURNAL: Section: E, Section No. 358, Vol. 09, No. 288, Pg. 140,
November 15, 1985 (19851115)

ABSTRACT

PURPOSE: To obtain an IC **element** having high **resistance** to radiation by a method in which, before separating an MIS-type IC element, the periphery of the element is surrounded by a thick **insulation film**, a thin gate **oxide film** is provided in an element forming region, an annular shield electrode is formed on the gate **oxide film**, and a region having the same type of conductance with the substrate and a high impurity concentration is provided under the shield *****electrode***** through the *****gate***** *****oxide***** *****film*****

CONSTITUTION: A thin SiO(sub 2) film 33 is adhered on the surface of a P type Si substrate 31. Ions are implanted into the periphery of the substrate to form a P(sup +) type region 32. An Si(sub 3)N(sub 4) film 35 is then provided on the film 33 such that the both ends thereof overlap with the regions 32. The substrate is heat treated to change the uppermost layer of the region 32 into a thick field SiO(sub 2) film 36, while the inner end of the region 32 is caused to penetrate in the **active ***region*****. After that, the film 35 required no more is removed and the film 33 connected to the film 36 is renewed to a gate **oxide film** 33', on which an annular shield electrode 37 is provided and covered with an SiO(sub 2) film connected to the films 36 and 33'. A *****gate***** *****electrode***** 38 is then adhered on the electrode 37. In such a manner, an IC **element resistant** to ionizing radiation can be obtained.

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26/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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00161869 INSPEC Abstract Number: B70027292

Title: Monolithic thin-film devices with **active** and resistive regions

Inventor(s): Currin, C.G.; Herczog, A.; Settzo, R.J.

Assignee(s): Corning Glass Works

Patent Number: US 3474304 Issue Date: 691021

Application Date: 680103

Priority Appl. Number: US 695435

Country of Publication: USA

Language: English

Abstract: An integrated circuit including a diode or non-linear circuit element and a **resistor** both formed by utilizing the same material, a mixture of tin oxide and antimony oxide. These two elements are formed in a single step by depositing on a semiconductor wafer a **film** of tin oxide and antimony oxide in such a manner that a portion of the film which is to form the diode contacts the semiconductor wafer, and the portion of the film which is to form the resistor is **insulated** from the semiconductor. To complete the diode an ohmic (metallic) contact is made to the semiconductor wafer near the area at which the film contacts the semiconductor.

Subfile: B

26/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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004470999

WPI Acc No: 1985-297877/198548

XRPX Acc No: N85-221766

Input protective circuit for integrated circuit - has channel length of protective transistor varied across width so that length at centre is shorter than peripheral regions

Patent Assignee: NEC CORP (NIDE)

Inventor: SATO Y

Number of Countries: 005 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 162460	A	19851127				198548 B
JP 60246665	A	19851206	JP 84102865	A	19840522	198604
US 4739438	A	19880419	US 85736728	A	19850522	198818
EP 162460	B	19910828				199135
DE 3583886	G	19911002				199141

Priority Applications (No Type Date): JP 84102865 A 19840522

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 162460	A	E	16		

Designated States (Regional): DE FR GB

EP 162460 B

Designated States (Regional): DE FR GB

Abstract (Basic): EP 162460 A

A protective transistor is coupled between a reference potential and part of the path between an input terminal and the gate of a functional transistor. The gate of the protective transistor is connected to the reference potential through a resistor, the latter being connected to the input transistor at its gate and to the reference terminal at its source or vice-versa.

The protecting transistor assumes a conducting state when an excessive or surge voltage is applied to the input terminal to discharge that voltage to the reference potential. The channel length of the protective transistor is varied along its width such that a length at a centre portion of the channel is shorter than that at both peripheral regions.

ADVANTAGE - Current flowing through channel is concentrated on centre portion to reduce current density near field oxide

layer , potential at gate of protective transistor raised quickly.

4/4

Abstract (Equivalent): EP 162460 B

A semiconductor device comprising an input terminal (31), an input transistor (3), a **resistive element** (4') coupled between the gate (32) of said input transistor and said input terminal, a protecting transistor (2), first means (15', 16') for electrically connecting one (12') of drain and source of said protecting transistor to the gate (32) of said input transistor, second means (14', 17') for electrically connecting the other (11') of said drain and source of said protecting transistor to a reference voltage terminal (GND), a resistor (5) coupled between the gate of said protecting transistor and said reference voltage terminal, said input transistor and protecting transistor being formed on **active regions** surrounded by a field **insulating layer** (19'), characterized in that the channel length (LS) around a center portion of said protecting transistor is made shorter than the other portions (LL) thereof and that a contact hole (16') for allowing a connection to said one (12') of drain and source of said protecting transistor is formed only at a center portion of said one of drain and source of said protecting transistor. (7pp)

Abstract (Equivalent): US 4739438 A

The protective transistor arrangement for MIS circuits and the like which is capable of stable operation without breakdown in the event of a surge voltage. The protective transistor has a channel region whose length varies along the width of the channel such that the channel length at the central portion of the channel region is made less than the channel length at the sides of the channel region.

By way of this construction, the current path through the protective transistor is largely confined to the central area of the channel region, preventing current from being concentrated at side portions of the channel region adjacent the field oxide surrounding the transistor. (8pp)e

26/3,AB/3 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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003696713

WPI Acc No: 1983-56695K/198324

XRAM Acc No: C83-055052

XRPX Acc No: N83-102502

High speed semiconductor device - has polysilicon wiring layer with metal doped or covered regions

11/14/2003

09/960,495

Patent Assignee: TOKYO SHIBAURA DENKI KK (TOKE)

Inventor: KONISHI S

Number of Countries: 005 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 80730	A	19830608	EP 82111033	A	19821130	198324 B
JP 58093347	A	19830603				198328
US 4604641	A	19860805	US 82445247	A	19821129	198634
EP 80730	B	19870923				198738
DE 3277393	G	19871029				198744

Priority Applications (No Type Date): JP 81192228 A 19811130

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 80730	A	E	27		
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Designated States (Regional): DE FR GB

EP 80730	B	E			
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Designated States (Regional): DE FR GB

Abstract (Basic): EP 80730 A

Semiconductor device comprises (a) a semiconductor substrate having an **active region** including a buried contact and a field region including a field **insulation** layer; (102) (b) a first polySi layer (105) formed in an **active region** and on the field **insulation** layer; and (c) a second polySi layer (111) having one portion formed directly on the first polySi layer and a second portion formed on an **isolation film** (108) covering part of the first polySi layer, the portion of the second polySi **layer** above the field **isolation layer** being metal doped (114) or covered by a metal film.

The device is made by (i) forming a first polySi layer contacting a buried contact area contacting a semiconductor substrate; (ii) forming a second polySi layer, partly on the first polySi layer with metal ats. or forming a metal film on its surface.

The structure may be used for substrates contg. MOS or bipolar devices, giving high packing density and low resistance for high speed operation. The second layer may serve as an additional wiring layer and/or *****resistor***** *****element*****.

4D/8

26/3,AB/4 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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002531487

WPI Acc No: 1980-49514C/198028

Related WPI Acc No: 1979-D6224B

Resistor elements for MOS integrated circuits - formed by ion implantation in a polycrystalline silicon layer

Patent Assignee: TEXAS INSTR INC (TEXI)

Inventor: LIEN J C; RAO G R M; STANCZAK J S

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4208781	A	19800624				198028 B

Priority Applications (No Type Date): US 78916037 A 19780615; US 76727116 A

EIC2800

Irina Speckhard

308-6559

19760927; US 80162217 A 19800623

Abstract (Basic): US 4208781 A

Resistor elements and interconnections in an integrated circuit are made by: forming an **insulating** coating on a semiconductor body surrounding active element areas of the surface of the body; depositing pure polycrystalline Si over the coating and at least some of the areas; implanting impurity into the polycrystalline Si to form resistor regions of lower resistivity than the polycrystalline Si; and introducing impurity into other polycrystalline Si regions at a higher concn. to form connections between the resistor **regions** and the **active** elements and between circuit elements.

Pref. the active elements are IGFETs with the polycrystalline Si forming gates; the *****insulating***** *****coating***** is pref. field **oxide** surrounding the transistors, with a much thinner **oxide ***layer***** underlying the gates.

*****Resistor***** *****elements***** are esp. useful for load devices in static RAM cells in MOS memory devices. The *****resistor***** **elements** are made by an ion implant step compatible with a self-aligned N-channel Si gate process.

26/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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06763293
MANUFACTURE OF SEMICONDUCTOR DEVICE WITH ELEMENT ISOLATION
INSULATING FILM

PUB. NO.: 2000-349164 [JP 2000349164 A]
PUBLISHED: December 15, 2000 (20001215)
INVENTOR(s): SHIMIZU MASAKUNI
APPLICANT(s): NEC CORP
APPL. NO.: 11-161682 [JP 99161682]
FILED: June 08, 1999 (19990608)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method of manufacturing a semiconductor device provided with an element **isolation insulating film**, where the surface of a substrate is covered with an oxidation-resistant film such as a nitride film or the like until the oxidation of a gate is started so as to prevent a useless **oxide film** from being formed on the substrate when a gate **oxide film** of different thickness is formed, and etching carried out before the oxidation of a gate can be reduced.

SOLUTION: In this manufacturing method, a semiconductor substrate 100 is equipped with element regions 501 and 502 where element isolation oxide films 101 and thin **oxide films** 201 each located on an **active region** between the **oxide films** 101, an oxidation-resistant film 301 is formed on all the surface of the semiconductor substrate 100, the semiconductor substrate 100 is exposed using a resist film 401 as a mask, where the element region 501 is not covered with the resist film 401, a first gate **oxide film** is formed, furthermore the semiconductor substrate 100 is exposed using a **resist film** where the **element** region 502 is open as a mask, and a second gate *****oxide***** *****film***** is formed.

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26/3,AB/6 (Item 2 from file: 347)
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05791794

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 10-074894 [JP 10074894 A]
PUBLISHED: March 17, 1998 (19980317)
INVENTOR(s): SONODA YASUHIRO
APPLICANT(s): NEC KYUSHU LTD [423996] (A Japanese Company or Corporation),
JP (Japan)
APPL. NO.: 08-228922 [JP 96228922]
FILED: August 29, 1996 (19960829)

ABSTRACT

PROBLEM TO BE SOLVED: To shorten a process for manufacturing a semiconductor device by a method, wherein a first diffusion layer and a silicide layer are made to serve as the terminal regions of a **resistive element**, and a second diffusion layer is made to function as the resistive part of the *****resistive***** *****element*****.

SOLUTION: A gate-**insulating** film 9 and a side wall **insulating** film 10 are laminated on a region of the surface of a silicon substrate 1, where an element **isolation insulating film** 2 is not formed or the center of an *****element***** *****active***** *****region*****. A **resistor** diffusion layer 5 is formed on the side wall **insulating** film 10 in a self-aligned manner, furthermore a pair of first impurity diffusion layers 11 are formed on both the edges of the element **active region**, and a silicide layer 6 is formed only on the impurity diffusion layers 11 respectively, so as to serve as terminal regions of a *****resistive***** *****element*****. A *****resistive***** diffusion layer 5 formed between the first impurity diffusion layers 11 to serve as a second diffusion layer is made to function as a resistor region of a *****resistive***** *****element*****. By this setup, a resistive element which is shortened in manufacturing process and suitable for high integration can be realized.

26/3,AB/7 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
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03048147

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 02-023647 [JP 2023647 A]
PUBLISHED: January 25, 1990 (19900125)
INVENTOR(s): HORIUCHI KATSUTADA
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 63-172660 [JP 88172660]

EIC2800

Irina Speckhard

308-6559

11/14/2003

09/960,495

FILED: July 13, 1988 (19880713)
JOURNAL: Section: E, Section No. 912, Vol. 14, No. 168, Pg. 7, March
30, 1990 (19900330)

ABSTRACT

PURPOSE: To obtain a highly accurate **resistance element** which has low parasitic capacitance and high breakdown strength and then, cuts off the occurrence path of α ray soft errors by making desired regions have the first and second *****insulating***** films.

CONSTITUTION: Desired regions which are provided at least at two places on a single crystal substrate 1 are equipped with the first **insulating films** 5 which are **isolated** by the single crystal substrate and are in contact with parts of side walls of the desired regions and, then, reach the single crystal substrate and, further, are perpendicular to the single crystal substrate as well as the second **insulating film** 8 which are prepared at the bottom face of the desired *****regions*****. Accordingly, **active** elements, such as a transistor and the like are constructed by causing them to be adjacent to the foregoing *****insulating***** films. Further, once a resistance is manufactured as a semiconductor **element**, a **resistance element** which is not very much dependent upon an operating temperature in the same way as that found for the **resistance elements** in conventional semiconductor substrates is obtained. Moreover, the region of the *****resistance*** element** is regulated by **insulators** 6 and deeply grooved **insulating films** 5 filling horizontal and vertical pits 8 and 5; besides, its region is isolated completely from the semiconductor substrate. In this way, the depth of an impurity diffusion layer is not expanded by heat treatment during a manufacturing process and an introduction path of α ray soft errors is cut off completely.

26/3,AB/8 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
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02296262

RADIATION-RESISTANT MIS TYPE SEMICONDUCTOR DEVICE

PUB. NO.: 62-213162 [JP 62213162 A]
PUBLISHED: September 19, 1987 (19870919)
INVENTOR(s): MIYAMOTO MASABUMI
YOSHIDA ISAO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 61-054717 [JP 8654717]
FILED: March 14, 1986 (19860314)
JOURNAL: Section: E, Section No. 587, Vol. 12, No. 69, Pg. 157, March
03, 1988 (19880303)

ABSTRACT

PURPOSE: To draw holes to a region unrelated to element characteristics from a gate region, and to improve the radiation-**resistant** performance of an **element** by forming a substance (a getter) having high trap density and a large number of recombination centers near an *****insulating***** gate.

CONSTITUTION: A thermal **oxide film** 3 and a gate 5 are formed through a normal MOSFET manufacturing process, source-drain regions 2 are

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shaped through ion implantation, sections except the thermal oxide film 3 just under the gate 5 are removed through etching, using the gate 5 as a mask, and glass PSG 4 is deposited as a getter. The thermal oxide film having excellent quality is formed onto an active region in which an MOS inversion layer is shaped, thus deteriorating no element characteristics. Holes generated by radiation exposure are drawn to the PSG film 4 from a section just under the gate 5, thus realizing an MOSFET, characteristics thereof are hardly deteriorated by radiation. An ***insulating*** film having a large number of traps and recombination centers may be used as the getter, and silicon nitride, etc. may also be employed.

26/3,AB/9 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
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02241455
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 62-158355 [JP 62158355 A]
PUBLISHED: July 14, 1987 (19870714)
INVENTOR(s): MITSUMOTO KAZUFUMI
HASEGAWA TERUO
APPLICANT(s): ROHM CO LTD [365425] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 60-299088 [JP 85299088]
FILED: December 31, 1985 (19851231)
JOURNAL: Section: E, Section No. 568, Vol. 11, No. 396, Pg. 108,
December 24, 1987 (19871224)

ABSTRACT

PURPOSE: To reduce the area of a substrate by forming an element annexed to an active element onto an active element region shaped to the substrate through an ***insulating*** means.

CONSTITUTION: A base region 4 having a reverse conduction type is formed to a P-type or N-type semiconductor substrate 2 through the diffusion, etc. of an impurity, and an emitter region 6 having a conductive type reverse to the base region 4 is shaped selectively to one part of the surface layer of the base region 4. An ***oxide*** ***film*** 22 ***coating*** the surface of the semiconductor substrate 2 is formed, openings 24, 26 are shaped selectively, and electrodes 14, 16 are shaped while an electrode 18 is also formed onto the surface of the ***oxide*** ***film*** 22. A protective film 32 as an insulating layer coating the electrodes 14, 16, 18 and the surface of the oxide film 22 is shaped, and openings 34, 36, 38 for wire bonding are formed selectively to the protective film 32. Resistance elements 10, 12 are shaped onto the protective film 32 in the upper surface section of the base region 4 as annexed elements by polysilicon, etc.

26/3,AB/10 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO
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02039749

SEMICONDUCTOR DEVICE

PUB. NO.: 61-253849 [JP 61253849 A]
PUBLISHED: November 11, 1986 (19861111)
INVENTOR(s): HIRAKAWA KAZUYOSHI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation)
, JP (Japan)
APPL. NO.: 60-095010 [JP 8595010]
FILED: May 02, 1985 (19850502)
JOURNAL: Section: E, Section No. 494, Vol. 11, No. 104, Pg. 147, April
02, 1987 (19870402)

ABSTRACT

PURPOSE: To enable to reduce a chip by a method wherein the **resistance elements**, which are parts of the electrostatic protection unit, are formed of diffusion layers to be formed under the element *****isolation***** *****layers*****.

CONSTITUTION: A semiconductor substrate 101 is oxidized by heat and after a silicon nitride film is formed thereon, an etching is performed to the silicon nitride film in the desired pattern. A resist is applied thereon, the part alone of a diffusion layer 102 for protective **resistance element** is opened and an impurity different from that of the substrate in type is implanted by an ion-implantation method. After that, a thermal oxidation is performed, element **isolation layers** 103 are formed, ions are implanted in the **activating regions**, diffusion layers 104 are formed and after an interlayer **insulating** film 105 is evaporated, contact holes are opened, wiring metal layers 106 are formed, a protective film 107 is evaporated and a wiring lead-out 108 is opened. By this way, a method-wherein the area needed for the **resistance elements**, which are parts of the electrostatic protection unit, is not increased-can be obtained even when the diffusion layers and the wiring are decreased in resistance.

26/3,AB/11 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO
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01492662

POLYCRYSTALLINE SILICON RESISTANCE ELEMENT

PUB. NO.: 59-204262 [JP 59204262 A]
PUBLISHED: November 19, 1984 (19841119)
INVENTOR(s): NISHISAKA TEIICHIROU
GOTO HIDETO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 58-078984 [JP 8378984]
FILED: May 06, 1983 (19830506)
JOURNAL: Section: E, Section No. 304, Vol. 09, No. 65, Pg. 114, March
26, 1985 (19850326)

ABSTRACT

PURPOSE: To eliminate the phosphorus diffusion to the titled element by electrically connecting said element to the other element via diffused region formed on a semiconductor substrate.

CONSTITUTION: A non-active region 11 is formed in the P type semiconductor substrate 10, a field insulation oxide film

12 is formed, and a window opened part 14 is bored in an insulation film 13. Next, after growing polycrystalline Si over the entire surface of the substrate, a polycrystalline Si layer containing high concentration phosphorus is formed, and next a wiring part 15 is formed. Then, the diffused part 17 is formed. The impurity concentration is all uniform except that of a window opened part 18, therefore the effective resistance length $l(\text{sub } 0)$ is almost dependent on the etching accuracy of said part 18. Thereby, the titled element can be manufactured with good reproducibility.

26/3,AB/12 (Item 8 from file: 347)
 DIALOG(R)File 347:JAPIO
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01007239

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 57-157539 [JP 57157539 A]
 PUBLISHED: September 29, 1982 (19820929)
 INVENTOR(s): TOKUMARU SEIYA
 NAKAI MASANORI
 APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
 (Japan)
 APPL. NO.: 56-042897 [JP 8142897]
 FILED: March 24, 1981 (19810324)
 JOURNAL: Section: E, Section No. 149, Vol. 06, No. 259, Pg. 110,
 December 17, 1982 (19821217)

ABSTRACT

PURPOSE: To integrate $I(\text{sup } 2)L$, a linear element and a bipolar element on a single substrate by selectively forming a buried layer having the structure of laminating or a single layer to the Si substrate and an epitaxial layer under an ***active*** ***region***.

CONSTITUTION: $N(\text{sup } +)$ layers 4a-4c are buried onto the P type Si substrate 2, the N epitaxial layer 6 is stacked, $N(\text{sup } +)$ layers 8a, 8b are stacked onto the layers 4a, 4b, an $N(\text{sup } +)$ epitaxial layer 10 is laminated, and the epitaxial layers are isolated by P layers 12, 14, 16, 18 reaching the substrate 2. $P(\text{sup } +)$ layers 30, 32 and 50, 52, 60 are formed simultaneously, $N(\text{sup } +)$ layers 38, 40 and 54, 62, 64 are shaped, and the junction regions of the $P(\text{sup } +)$ layer 32 and P layers 34, 36 are used as the ***resistors*** of ***element*** sections 22, 24. According to this constitution, the amount of holes stored decreases because an $N(\text{sup } +)$ layer 10a is thin in the $I(\text{sup } 2)L$ 10, speed is increased, a current amplification factor is augmented, and integration can be heightened. Since an $N(\text{sup } +)$ layer 10b is thin in the bipolar element 22, speed is increased, series resistance is low, and output voltage at the time of saturation is low. With the linear element 24, the epitaxial layer can be laminated in desired thickness, a layer such as a layer 6c is thickened, concentration is kept at low concentration regardless of regions 20, 22, and ***dielectric*** resistance can be increased.

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31/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013522127

WPI Acc No: 2001-006333/200101

Related WPI Acc No: 2000-136470; 2001-289739; 2002-163024

XRAM Acc No: C01-001377

XRFX Acc No: N01-004510

Capacitor storage node forming method for fabrication of DRAM, involves removing portion of BPSG layer by anisotropic dry etching to form elongated stem-like openings of minimum photolithographic dimension

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: PAREKH K R

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6140172	A	20001031	US 97798251	A	19970211	200101 B
			US 98204749	A	19981202	

Priority Applications (No Type Date): US 97798251 A 19970211; US 98204749 A 19981202

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6140172	A	32	H01L-021/8234	Div ex application	US 97798251

Abstract (Basic): US 6140172 A

Abstract (Basic):

NOVELTY - A borophosphosilicate glass (BPSG) layer (34a) is formed on a semiconductor substrate at nodal areas (25a,27a,29a). The portions of BPSG layer masked and unmasked by polysilicon layer, are removed by anisotropic dry etching and subsequent isotropic wet etching to form a tapered elongated stem-like openings having dimensions lesser than minimum photolithographic dimensions.

DETAILED DESCRIPTION - Undoped polysilicon masking layer is patterned on BPSG layer (34a). INDEPENDENT CLAIMS are also included for the following: (i) Capacitor forming method which involves forming a sacrificial silicon **oxide layer** over an etch restriction layer (102) within the tapered elongate stem-like openings. Doped polysilicon pedestals (116b-118b) extending into the BPSG layer, are formed in the openings, after etching the etch restriction layer and BPSG layer (34a). The sacrificial layer is removed to form gap between the lateral surfaces of the pedestals and the BPSG layer. A storage node layer, is formed adjacent the lateral surfaces of the pedestal and a masking layer is formed over the node layer. The unmasked portion of the node layer is removed and the node *****layer***** is *****polished*****. A dielectric **layer** and a cell plate layer are formed adjacent the node layer to form the capacitor; (ii) Bitline construction method which involves forming the stem-like openings underlying the BPSG layer, not extending to the nodal areas and forming another pair of openings extending from the prior set of openings to the nodal areas by removing portion of the BPSG and the sacrificial layers. Gap is formed between the BPSG layer and the pedestals and storage node layer, dielectric layer and cell plate layer are formed in the gap. Another BPSG layer is formed over the prior BPSG layer and the pedestals. Portion of the secondary BPSG layer in one of the gaps is removed to expose the pedestals and the capacitor layers. The pedestal and the

capacitor layers are partially removed. An electrically conductive bitline plug is formed in electrical connection with the exposed pedestal; (iii) DRAM array construction method which involves forming bitlines over the capacitors formed in the gap between pedestal and the BPSG layer (34a), where the exposed pedestal and the capacitor connected to the bitlines form the DRAM cell; (iv) Monolithic integrated circuit forming method which involves forming capacitor, transistor and **resistive elements** on the semiconductor substrate in which the transistor gate (26a) electrically couples the nodal areas.

USE - For fabrication of DRAM cell used in microprocessor.

ADVANTAGE - The etching of the BPSG layer and the etch restriction layer before pedestal formation, ensures adequate clearance around upper corners of the pedestals for subsequent capacitor formation.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the wafer fragment during DRAM cell construction.

Nodal areas (25a,27a,29a)

Transistor gate (26a)

Borophosphosilicate glass layer (34a)

Etch restriction layer (102)

Doped polysilicon pedestals (116b-118b)

pp; 32 DwgNo 22/22

31/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013087842

WPI Acc No: 2000-259714/200023

XRAM Acc No: C00-079695

XRPX Acc No: N00-193257

Planarization of **oxide film** for manufacturing semiconductor device, involves implanting phosphorus ion using resist **film** as mask before **polishing** process

Patent Assignee: NIPPON STEEL CORP (YAWA)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11340174	A	19991210	JP 98164212	A	19980528	200023 B

Priority Applications (No Type Date): JP 98164212 A 19980528

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 11340174	A	4	H01L-021/304	

Abstract (Basic): JP 11340174 A

NOVELTY - Multiple transistor elements (TR) are formed on a semiconductor substrate (11). An *****oxide***** *****film***** (12) is formed on the substrate. The phosphorus ion is implanted into the *****oxide***** **film** via a resist film (13) which is formed on a recess in

*****oxide***** *****film***** as a mask. Then, the *****oxide***** *****film***** is

*****polished*****

USE - For manufacturing semiconductor device.

ADVANTAGE - Flat **oxide film** is obtained irrespective of its background pattern by uniform **polishing** process, since the **layer** insulation film is not dependent on the roughness and

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fineness of element pattern formed on semiconductor substrate.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of
processes involved in semiconductor device manufacture. (11)
Semiconductor substrate; (12) **Oxide** film; (13) **Resist**
film ; (TR) Transistor ***elements***
Dwg.1/5

31/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010100882

WPI Acc No: 1995-002135/199501

XRAM Acc No: C95-000850

XRPX Acc No: N95-001856

Prepn. of magneto-resistance effect type magnetic head - by laminating a
polycrystalline ferrite substrate, an insulating layer, a soft magnetic
film, etc., for magnetic disc device

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 6290424	A	19941018	JP 9373203	A	19930331	199501 B

Priority Applications (No Type Date): JP 9373203 A 19930331

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 6290424	A	4	G11B-005/39	

Abstract (Basic): JP 6290424 A

Method is effected by lamination of a polycrystalline ferrite
substrate, an insulating layer of which **surface** is **polished**
, a soft magnetic **film**, an intermediate layer having magneto
resistance effect **element** and diaferromagnetic film with
lead portion at the both ends, an **oxide layer**, lower
magnetic **layer** with magnetic gap portion and a Cu coil portion
for write, an insulating layer and an upper magnetic layer in that
order.

USE/ADVANTAGE - The head is suitable for magnetic disc device. It
has improved reliability, since the films and layers have improved
running life by ***polishing*** ***surface*** of the insulating layer.
Dwg.2/6

31/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009896377

WPI Acc. No: 1994-176293/199421

Related WPI Acc No: 1994-316282

XRAM Acc No: C94-080698

XRPX Acc No: N94-138849

Prod'n. of multi-value linear resistors for IC using single mask level -
includes using number of trenches of specified lateral dimensions which
are filled with 2 conductive layers of high and low resistivity and a
dielectric layer and planarised

11/14/2003

09/960,495

Patent Assignee: NORTHERN TELECOM LTD (NELE)
Inventor: BOYD J M; ELLUL J P; TAY S P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5316978	A	19940531	US 9337048	A	19930325	199421 B

Priority Applications (No Type Date): US 9337048 A 19930325

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

US 5316978 A 15 H01L-021/3205

Abstract (Basic): US 5316978 A

A multi-valued linear resistors for an integrated circuit is obtd. using a single mask level a number of trenches are defined in a substrate. Each *****trench***** has contact regions of a sp0ecific lateral dimension and a narrower portion extending between them successive conformal layers of a first dielectric layer, a first conductive layer of high resistivity and a second conductive layer of lwoer resistivity are provided to fill the *****trench*****. The amt. of the second conductive layer which fills the **trench** depends on the width of the *****trench*****. The resulting structure is planarised, pref. by **chemical mechanical polishing** ot provide fully planarised topography.

When the first and second conductive layers are provided from layers of undoped and doped polysilicon respectively, the **trench** dimensions control the amt. of dopant incorporated in each region of the treench. After annealing to diffuse the dopant, the wider end contact regions are heavily doped to form contact regions, and the intermediate narrow portion of the **trench** is doped to a level dependent on the width of the **trench**, thereby forming a **resistive element** having a **resistivity** inversely dependent on the *****trench***** width.

ADVANTAGE - The method is compatible with CMOS, Bipolar and Bipolar CMOS processes.

Dwg. 6a-c/8

31/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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07392743

SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

PUB. NO.: 2002-261244 [JP 2002261244 A]
PUBLISHED: September 13, 2002 (20020913)
INVENTOR(s): AMISHIRO HIROYUKI
KUMAMOTO TOSHIO
IGARASHI MOTOSHIGE
YAMAGUCHI KENJI
APPLICANT(s): MITSUBISHI ELECTRIC CORP
APPL. NO.: 2001-059948 [JP 20011059948]
FILED: March 05, 2001 (20010305)

ABSTRACT

PROBLEM TO BE SOLVED: To improve reliability, by forming **resistance elements** having desired shapes on an element **isolating ***oxide*** ***film***** and enhancing the precision of a resistance value.

EIC2800

Irina Speckhard

308-6559

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SOLUTION: In this semiconductor device, in which a plurality of the **resistive elements 4** are formed on the **element isolating oxide film 2** in a prescribed region formed on the surface of a semiconductor substrate 1, active regions 3 are arranged at positions adjacent to the *****resistance***** *****elements***** 4. Thereby the **element isolating oxide film 2** in the vicinities of the **resistance elements 4** can be partitioned in necessary regions, and the formation of a recessed part in a central part of the **element isolation oxide film 2** can be restrained, when the **film 2** is **polished** by a **CMP** method, so that the dimensional accuracy of the shapes of the **resistive elements 4** can be improved.

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31/3,AB/6 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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06570642
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 2000-156420 [JP 2000156420 A]
PUBLISHED: June 06, 2000 (20000606)
INVENTOR(s): MIYAHARA SUSUMU
APPLICANT(s): NEC CORP
APPL. NO.: 10-330691 [JP 98330691]
FILED: November 20, 1998 (19981120)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce a difference between the depths of contact holes which are formed on a *****resistance***** *****element***** and a device.

SOLUTION: A device, such as a transistor, is formed in a silicon substrate 1. An oxide *****film***** 2, a nitride *****film***** 3 and an *****oxide*****

film 4 are laminated in order on the substrate 1 formed with the device to form the films 2, 3 and 4. A groove for forming a **resistance element 8** in a prescribed region of the **film 4** is formed in the **film 4**. A nitride film 5 having a film thickness in the extent that the groove is not filled with the **film 5** is formed on the **film 4** formed with the groove. A polycrystalline silicon film is formed on the **film 5**, and the polycrystalline silicon **film** is **polished** using the **film 5** as a stopper to form the **resistance element 8** in the prescribed region of the *****film***** 4. An *****oxide***** *****film***** 9

and a BPSG film 10 are laminated on the **film 5** formed with the **element 8** to form the films 9 and 10 on the **film 5**, and contact holes 11 are formed on the **element 8** and the device to provide a wiring.

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31/3,AB/7 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
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06412742

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 11-354400 [JP 11354400 A]
PUBLISHED: December 24, 1999 (19991224)
INVENTOR(s): SAINO KANTA
APPLICANT(s): NEC CORP
APPL. NO.: 10-164719 [JP 98164719]
FILED: June 12, 1998 (19980612)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent drop of alignment precision by allowing at least a part of the alignment mark provided on a substrate to protrude above a substrate surface.

SOLUTION: A nitride film 3 is formed on a pad oxide film 2 formed on an Si substrate 1, on which a photo-resist element separation pattern is formed. Then, the nitride film 3 and the pad oxide film 2 are sequentially ion-etched, reactive anisotropically, to expose the Si substrate 1. Then, after the photo-resist is released, the Si substrate 1 is anisotropically etched with the nitride film 3 as a mask to form a groove 4. Then, with the nitride film 3 as a mask, the Si substrate 1 is thermally oxidized to form a thermal oxide film 5 on a side wall and a bottom surface of the groove 4. Then a CVD ***oxide*** ***film*** 6 is deposited to bury the groove 4 appropriately, and CMP is so performed as to expose the nitride film 3 for flattened CVD ***oxide*** ***film*** 6. Then, etching is performed using a mask wherein a photo-resist 7 is patterned, to adjust the height of the upper surface of the CVD ***oxide*** ***film*** 6.

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31/3,AB/8 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
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06356092

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURE

PUB. NO.: 11-297700 [JP 11297700 A]
PUBLISHED: October 29, 1999 (19991029)
INVENTOR(s): NOGUCHI JUNJI
YAMAGUCHI HIDE
OWADA NOBUO
APPLICANT(s): HITACHI LTD
APPL. NO.: 10-104629 [JP 98104629]
FILED: April 15, 1998 (19980415)

ABSTRACT

PROBLEM TO BE SOLVED: To surely avoid corrosion of metal wirings or metal plugs formed by the COMPONENTS method.

SOLUTION: A light shield layer 20 of e.g. a Cu film is formed above p-type semiconductor regions 4 constituting terminal resistance elements R, at the same time as a step of polishing the Cu film deposited to an upper part of an Si oxide film 21 by

the **CMP** method to form second layer wirings 17-19, and has a wide area enough to cover approximately the entire p-type semiconductor region 4. By placing the light shield layer 20 above the p-type semiconductor region 4, the light incidence on the p-type semiconductor region 4 can be avoided in the step of **polishing** the Cu film by the **CMP** method to form the second layer wirings 17-19, and the corrosion of the wirings 17-19 due to a photo current generated by a light incident on the p-n junction is avoided.

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31/3,AB/9 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
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05375141

SUPERCONDUCTING ELEMENT AS WELL AS ITS MANUFACTURE AND OPERATING METHOD

PUB. NO.: 08-330641 [JP 8330641 A]
PUBLISHED: December 13, 1996 (19961213)
INVENTOR(s): TARUYA YOSHINOBU
SUGII NOBUYUKI
FUKAZAWA TOKUMI
KABASAWA TAKANORI
HASEGAWA HARUHIRO
TAKAGI KAZUMASA
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 07-134886 [JP 95134886]
FILED: June 01, 1995 (19950601)

ABSTRACT

PURPOSE: To obtain a superconducting element whose circuit constitution and operating system are simplified and which can be operated at high speed by a method wherein a gate voltage which is applied to a gate electrode is used as an input signal as well as a tunnel resistance value and a superconducting current value are controlled.

CONSTITUTION: (100) plane orientations of two strontium titanate single crystals are made to agree, the orientations are displaced by a prescribed angle inside a plane so as to be bonded, a bicrystal single crystal having a grain boundary 2 is cut at the (100) plane orientations, and a substrate 1 for a superconducting element is formed. The central part 3 on the rear of the substrate 1 is chemically **polished**, and a **surface** is formed as a mirror surface. Then, a Ba-K-Bi *****oxide***** thin *****film***** having a tunnel insulating layer 5 is formed on the surface. Then, a wiring pattern, a source electrode 4, a drain electrode 6, a **resistance element** and the like for the superconducting element are formed on the Ba-K-Bi *****oxide***** thin *****film*****. Then, an Au film is formed on the rear of the substrate 1, and a gate electrode 7 is formed. A tunnel resistance value and a current value are controlled by a gate voltage.

31/3,AB/10 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO
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04952834

WIRING FILM AND NONLINEAR RESISTOR ELEMENT AND THIN-FILM TRANSISTOR AND LIQUID-CRYSTAL DISPLAY AND SEMICONDUCTOR DEVICE AND MANUFACTURE OF WIRING FILM AND NONLINEAR RESISTOR ELEMENT AND THIN-FILM TRANSISTOR AND SEMICONDUCTOR DEVICE

PUB. NO.: 07-245434 [JP 7245434 A]
PUBLISHED: September 19, 1995 (19950919)
INVENTOR(s): INOUE TAKASHI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-032428 [JP 9432428]
FILED: March 02, 1994 (19940302)

ABSTRACT

PURPOSE: To manufacture high-quality wiring films without defects with less dispersion of quality by simple processes, by grinding a metal layer and forming an anode ***oxide*** ***film*** on the surface of the metal layer.

CONSTITUTION: A wiring film 12 is composed of elements including Ta being a main component. And the wiring film 12 patterned into a specified shape is electrolytically polished by making the film an anode, and applying voltage between the film and a cathode 10. An electrolytic solution used for the electrolytic polishing on this occasion is an aqueous solution containing 0.5-7% of hydrofluoric acid and 32-38% of hydrochloric acid, and the electrolytic polishing is performed by an impressed voltage 40-60V, and a current density 0.1-0.2A/cm(sup 2). After that, the substrate 11 is cleaned with pure water and the water is swished off. Then it is dipped in an anode oxidizable electrolytic solution, and an anode oxide film 13 is deposited on the surface of the wiring film 12. As a result of this, it becomes possible to obtain high-quality wiring films having few defects without quality dispersion by simple processes.

31/3,AB/11 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO
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03915536

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF.

PUB. NO.: 04-280636 [JP 4280636 A]
PUBLISHED: October 06, 1992 (19921006)
INVENTOR(s): TANI SATORU
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-043603 [JP 9143603]
FILED: March 08, 1991 (19910308)
JOURNAL: Section: E, Section No. 1322, Vol. 17, No. 85, Pg. 86, February 19, 1993 (19930219)

ABSTRACT

PURPOSE: To stabilize the contact, etc., between wirings by a method wherein the leading-out conductive layer, etc., of ***resistors*** and active elements are buried in field oxide films so that the field oxide films may be flush with the leading-out conductive layers, etc., of ***resistor*** and active ***elements***

EIC2800

Irina Speckhard

308-6559

CONSTITUTION: Field **oxide films** 2 are formed to leave active element region 4 parts by LOCOS step, etc., on an Si substrate 1 and then the field **oxide films** 2 are etched away to form resistance regions 3. Simultaneously with said steps, the peripheral parts exposing the Si substrate 1 are etched away to be expanded for the formation of the active element region 4 parts. Next, the first polycrystalline semiconductor layers 5 are formed on the whole surface of the Si substrate 1 and then the **surface** is **polished** so as to make the polycrystalline semiconductor layer 5 in the resistance regions 3 and the active element regions 4 flush with the field *****oxide***** *****films***** 2. Through these procedures, the surface where active **element**, **resistors** are formed can be flattened thereby enabling the stable contact, etc., between wirings to be made.

31/3,AB/12 (Item 8 from file: 347)
 DIALOG(R)File 347:JAPIO
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01779040
 PRODUCTION OF SEMICONDUCTOR DEVICE

PUB. NO.: 60-257540 [JP 60257540 A]
 PUBLISHED: December 19, 1985 (19851219)
 INVENTOR(s): SAKURAI HIROMI
 APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
 APPL. NO.: 59-115884 [JP 84115884]
 FILED: June 04, 1984 (19840604)
 JOURNAL: Section: E, Section No. 402, Vol. 10, No. 125, Pg. 100, May 10, 1986 (19860510)

ABSTRACT

PURPOSE: To provide an **element** having high pressure **resistance**, by a method in which a sputter **oxide film** is formed on the surface of a substrate to have a thickness of 5 μ m or more and is provided in a part thereof with an aperture, which is filled with a semiconductor grown epitaxially, and the upper face of the epitaxially grown **film** is **polished** to be flattened, so that an active region isolated by the sputter *****oxide***** *****film***** is provided.

CONSTITUTION: Boron is implanted in the upper face of a p type Si substrate 1 for forming a channel cut layer 2. Subsequently, a 11 μ m thick sputter SiO(sub 2) film 3a is formed thereon. The sputter SiO(sub 2) film 3a is then provided with an aperture 4, through which arsenic is implanted to form an n(sup +) type buried collector layer 5. After that, Si is caused to epitaxially grow selectively so as to have a thickness of about 12 μ m. The Si *****film***** is then *****polished***** to reduce the thickness to 10 μ m and to flatten the surface. In this manner, an active region isolated by the SiO(sub 2) film is obtained. Since the active region thus obtained has a thickness as large as 10 μ m, an element having a sufficiently high pressure resistance can be obtained.

31/3,AB/13 (Item 9 from file: 347)
 DIALOG(R)File 347:JAPIO
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01688848

MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 60-167348 [JP 60167348 A]
PUBLISHED: August 30, 1985 (19850830)
INVENTOR(s): IINO TERUO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 59-022244 [JP 8422244]
FILED: February 09, 1984 (19840209)
JOURNAL: Section: E, Section No. 371, Vol. 10, No. 1, Pg. 128, January
07, 1986 (19860107)

ABSTRACT

PURPOSE: To eliminate the failure of the chips due to crystal defect or the photo masks damaged by such protrusions as mounts and pits formed on the surface of the epitaxial layer and to upgrade the yield of the semiconductor device by a method wherein such **elements** as transistor, **resistor** and so forth are formed on the back surface of the semiconductor substrate with the main surface whereon the epitaxial layer has been formed.

CONSTITUTION: A prescribed part of an **oxide film 2** is selectively removed, N type impurities are diffused and an N type impurity region 4 is formed in such a way that the region 4 holds a constant plane-wise distance to P type impurity regions 3. At this time, P type silicon layers 5 grown on the **oxide film 2** left are turned into polycrystalline silicon layers and P type silicon layers 6 formed on the impurity diffusion regions 3 and 4 are turned into epitaxial layers. P type impurities are diffused up to reach the P type regions 3 from the prescribed parts 8, 8a and 8b on the **polished back surface 7a** of the N type silicon substrate 1. Lastly, P type impurity regions 10 and 10a and N type impurity regions 11 and 11a are formed in order in the back surface 7a of the N type silicon substrate 1, and P type **resistance** layers and such **elements** as N-P-N transistor and so forth are formed.

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33/3,AB/1 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS
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1666062 NTIS Accession Number: AD-A252 575/6

In vitro Corrosion Study of Two Implant Materials Using Electrochemical Impedance Spectroscopy and Potentiodynamic Polarization
(Master's thesis)

Kerber, M. W.

Air Force Inst. of Tech., Wright-Patterson AFB, OH.

Corp. Source Codes: 000805000; 012200

Report No.: AFIT/CI/CIA-92-023

1992 160p

Languages: English Document Type: Thesis

Journal Announcement: GRAI9220

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NTIS Prices: PC A08/MF A02

In vitro corrosion evaluations of commercially pure titanium (CP-Ti) and Ti-6Al-4V samples with different surface treatments were conducted using potentiodynamic polarization and electrochemical impedance spectroscopy (EIS). The different surface treatments tested were as-polished, nitric acid passivated (ASTM F86), and anodized. The test solution consisted of oxygenated 0.9 normal NaCl buffered to a pH of 7.3 at 37 deg C. The corrosion properties were shown to be similar for the two metals in the polished and passivated condition. The CP-Ti was found to be more corrosion resistant than the Ti-6Al-4V in the anodized condition. For both metals, the anodized condition was much more corrosion **resistant** than the **passivated** condition which was more corrosion resistant than the as-
polished condition. The ***oxide*** ***layer*** on both metals in the

as-polished and passivated conditions as well as on the CP-Ti in the anodized condition was composed of non-porous TiO₂. The protection provided by this layer was found to be related to its thickness. The oxide on the anodized Ti-6Al-4V was composed of a porous layer of hydrated TiO₃ on top of a nonporous layer of TiO₂. Although this layer was thicker than that on the anodized CP-Ti, it did not provide as much protection against corrosion.

33/3,AB/2 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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02203648 JICST ACCESSION NUMBER: 94A0885921 FILE SEGMENT: JICST-E

The Development of Ozone Oxidisation Treatment Method on Electro Chemical Buffing Stainless Steel for Clean System.

SHIMIZU SHIGEO (1); YAGI TAKAHARU (1); IWATA NOBUHIDE (1); SAWADA HIDETAKA (1); BABA YOSHIYASU (2)

(1) Hitachi Zosen Corp.; (2) Hitachiseimitsukenma

Hitachi Zosen Giho(Hitachi Zosen Technical Review), 1994, VOL.55,NO.3,

PAGE.197-202, FIG.14, TBL.1, REF.8

JOURNAL NUMBER: F0063AAW ISSN NO: 0018-2788 CODEN: HZOGA

UNIVERSAL DECIMAL CLASSIFICATION: 669:621.795

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

EIC2800

Irina Speckhard

308-6559

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: Corrosion resistance of stainless steel can be improved by forming stable Cr passivation film on the surface. In order to planning ultra-cleanup for semiconductor manufacturing equipment or surrounding machinery and tools, ozone oxidation treatment was developed for passivation of stainless steel **surface polished** like a mirror. And comparing with oxygen oxidation treatment, the following result was obtained. (1) Ozone oxidation treatment method enable the stable surface passivation at lower temperature and shorter time than oxygen oxidation treatment method. (2) By smooth surface and dense Cr passivation film, the quantity of gas release into ultra-high vacuum can be decreased. (3) Corrosion *****resistance***** of amorphous Cr **passivation** film formed at low temperature is the cause of decrease of quantity of release out metal ion into high temperature ultra-pure water. (author abst.)

33/3,AB/3 (Item 1 from file: 144)

DIALOG(R) File 144:Pascal

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10919519 PASCAL Number: 93-0428882

The effect of dry passivation treatments on the corrosion resistance, moisture release and structure of the surface **oxide film** on electropolished stainless steel

Passivation of metals and semiconductors. I, Passivity of metals, Sapporo, Japan, Sept. 24-28, 1989

TOMARI H; SATOH F; TERADA M; SATOH H; OHMI T; NAKAHARA Y

SATO Norio, ed; SUGANO Takuo, pref; HASHIMOTO Koji, ed

Kobe Steel Ltd, materials res. laboratory, Chuo-ku, Kobe 651, Japan

Hokkaido university, faculty english, Sapporo, Japan

Deutsche Bunsen-Gesellschaft fuer Physikalische Chemie, Frankfurt, Federal Republic of Germany.; Electrochemical Society, Princeton NJ, USA.;

Electrochemical Society of Japan, Japan.; Institute of Corrosion Science and Technology, Terra incognita.; Electron Devices Society. Institute of Electrical and Electronics engineers Inc., USA.; Institute of Electronics, Information and communication Engineers in Japan, Tokyo, Japan.; Iron and Steel Institute of Japan, Japan.; Japan Institute of Metals, Japan.; Japan Institute of Metals, Japan.; Japan Society of Applied Physics, Tokyo, Japan.

International symposium on passivity, 6 (Sapporo JPN) 1989-09-24

Journal: Corrosion science, 1990, 31 389-394

Language: English Summary Language: English

The objective of the present study is to investigate the effect of dry **passivation** treatments on corrosion **resistance**, moisture release behavior and structure of **oxide film** on electro-

*****polished***** Type 316L stainless steel. The corrosion resistance was evaluated by measuring the incubation time until H SUB 2 evolution occurred in HCl solution and the linear polarization resistance in boiling 0.005M-Na SUB 2 SO SUB 4 solution. The moisture release behavior was investigated by measuring the volume of H SUB 2 O desorption with ultra pure N SUB 2 gas purging

33/3,AB/4 (Item 1 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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015029551

WPI Acc No: 2003-090068/200308

XRAM Acc No: C03-022715

XRPX Acc No: N03-071094

Integrated circuit structure has wire bonded copper-pad copper-wire component having copper-pad bonded to copper-alloy wire which has self-passivation areas on dopant rich interface, and pad, bond and wire surfaces

Patent Assignee: INFINEON TECHNOLOGIES NORTH AMERICA CORP (INFN); BARTH H (BART-I); INFINEON TECHNOLOGIES AG (INFN)

Inventor: BARTH H

Number of Countries: 024 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020084311	A1	20020704	US 2000751479	A	20001228	200308 B
WO 200254491	A2	20020711	WO 2001US43960	A	20011114	200308
US 6515373	B2	20030204	US 2000751479	A	20001228	200313
EP 1348235	A2	20031001	EP 2001987076	A	20011114	200365
			WO 2001US43960	A	20011114	

Priority Applications (No Type Date): US 2000751479 A 20001228

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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US 20020084311	A1		7	B23K-031/00	
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WO 200254491	A2 E			H01L-023/488	
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Designated States (National): CN JP KR

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU

MC NL PT SE TR

US 6515373	B2			H01L-023/48	
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EP 1348235	A2 E			H01L-023/488	Based on patent WO 200254491
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Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI

LU MC NL PT SE TR

Abstract (Basic): US 20020084311 A1

Abstract (Basic):

NOVELTY - An integrated circuit structure has a wire bonded copper-pad (Cu-pad) Cu-wire component having a metallization-line, liner separating line and Cu-alloy surrounding the pad, dielectric surrounding the liner, and pad (11) bonded to Cu-alloy wire (10) having self-passivation areas on dopant rich interface (16) between alloy and liner, surfaces of pad and bond between pad and alloy wire, and alloy wire surface.

DETAILED DESCRIPTION - An integrated circuit structure has a wire bonded copper-pad (Cu-pad) Cu-wire component having a metallization-line, a liner separating metallization line and a Cu-alloy surrounding the pad, a dielectric surrounding the liner, and a Cu-pad (11) bonded to a Cu-alloy wire (10) having self-passivation areas on a dopant rich interface (16) between Cu-alloy and liner, Cu-pad surface, surface of bond between Cu-pad and Cu-alloy wire, and Cu-alloy wire surface.

An INDEPENDENT CLAIM is included for the preparation of integrated circuit structure having a wire bonded Cu-pad with Cu-wire component, which involves patterning a damascene structure in a dielectric to form wiring and bond pads, depositing a metallic liner, depositing Cu-alloy as seed-layer for final Cu-film, filling the damascene structure with pure Cu, pre-chemical mechanical polish (CMP) annealing at low temperature (less than 200degreesC), to form a low-resistive Cu-film

with large Cu-grains, and prevent out-diffusion of dopants in the Cu-alloy, Cu-CMP to remove Cu-overfill, and by liner CMP, post CMP annealing at 250-450degreesC to form a self-passivating dopant rich layer at the Cu-surface and at the Cu-liner interface, depositing a polyimide layer, patterning the polyimide and completing passivation by lithographic and etch steps to open the pad area to provide a clean Cu-surface for probing, probing the chips, wire bonding the probed pads with the Cu-alloy wires, and annealing the bonded chips at 250-450degreesC to form a self-passivating layer on the open Cu-pad surface and Cu-wire.

USE - As integrated circuit structure.

ADVANTAGE - The integrated circuit structure has Cu-wire bonded on Cu-pads which provides good bondability, good bond quality and low resistance coupled with the capacity of self-passivation, thereby

resisting corrosion and oxidation.

DESCRIPTION OF DRAWING(S) - The figure shows the Cu-alloy wire after wire bonding and annealing to a Cu-pad, in which the formed bond is either a ball or wedge, and in which there is a dopant rich interface layer characterized by self-passivation.

Cu-alloy wire (10)

Cu-pad (11)

Interface (16)

pp; 7 DwgNo 2/2

33/3,AB/5 (Item 2 from file: 350)
 DIALOG(R)File 350:Derwent WPIX
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009306274

WPI Acc No: 1992-433683/199252

XRAM Acc No: C92-192590

Forming corrosion **resistant passive** film on stainless steel -
 by electrolytic **polishing of surface**, oxidising in oxidative
 atmos. and removing iron *****oxide***** *****film***** by reduction with
 hydrogen@

Patent Assignee: OHMI T (OHMI-I); OSAKA SANSO KOGYO KK (OSAO); OMI T
 (OMIT-I)

Inventor: NAKAMURA M; OHMI T

Number of Countries: 018 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9221786	A1	19921210	WO 92JP699	A	19920528	199252 B
JP 4510159	X	19930603	JP 92510159	A	19920528	199327
			WO 92JP699	A	19920528	
EP 587893	A1	19940323	EP 92917389	A	19920528	199412
			WO 92JP699	A	19920528	
EP 596121	A1	19940511	EP 92917389	A	19920528	199419
			WO 92JP699	A	19920528	
EP 596121	A4	19941123	EP 92917389	A		199541
JP 10204526	A	19980804	JP 91212592	A	19910730	199841
JP 3045576	B2	20000529	JP 91212592	A	19910730	200030
JP 3181053	B2	20010703	JP 92510159	A	19920528	200139
			WO 92JP699	A	19920528	

Priority Applications (No Type Date): JP 91212592 A 19910730; JP 91152466 A
 19910528; JP 91198718 A 19910712

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9221786	A1	J	44	C23C-008/14	
Designated States (National): CA JP KR US					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LU MC NL SE					
JP 4510159	X		44	C23C-008/14	Based on patent WO 9221786
EP 587893	A1	E		C23C-008/14	Based on patent WO 9221786
Designated States (Regional): BE FR GB IT NL					
EP 596121	A1	E	35	C23C-008/14	Based on patent WO 9221786
Designated States (Regional): BE FR GB IT NL					
EP 596121	A4			C23C-008/14	
JP 10204526	A		15	C21D-001/76	
JP 3045576	B2		16	C21D-001/76	Previous Publ. patent JP 10204526
JP 3181053	B2		25	C23C-008/14	Based on patent WO 9221786

Abstract (Basic): WO 9221786 A

The process comprises subjecting the surface of the stainless steel to electrolytic polishing, oxidising in an oxidative atmos. and removing the iron oxide formed thereon by reduction with H₂. Stainless steel is furnished with a passive film having a surface roughness (R_{max}) of 0.1 micron or less. (pref. 0.01 micron or less). A gas- and liquid contacting part has a passive film formed on the stainless steel by the above mentioned process.

Pref. heat treatment at 300-600 deg.C in the atmos. of an inert gas performed between the electrolytic polishing and oxidation steps. In the H₂ treatment step for removal of the **oxide film** the concentration of H₂ contained in the gas is 0.1 ppm-10% and its temperature is 200-500 deg.C. After H₂ treatment, annealing is pref. conducted in the inert gas atmos. at 200-500 deg.C for 1-10 hrs. (pref. at 475 deg.C or higher). The atomic ratio of Cr/Fe on the surface of the passive film is larger than it is in the stainless steel (base material), and is pref. 1- or more. The gas- and liq-contacting part of the steel is pref. subjected to heat treat in an inert gas atmos. at 350-600 deg.C between the electrolytic polishing and oxidation steps.

USE/ADVANTAGE - Stainless steel having a passive film has excellent degasifiability and resistance against corrosion. It is useful for building ultra-high vacuum generating systems, ultra-clean depressurising systems, and ultra pure water generating systems a

Dwg.0/18

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35/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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07392743

SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

PUB. NO.: 2002-261244 [JP 2002261244 A]
PUBLISHED: September 13, 2002 (20020913)
INVENTOR(s): AMISHIRO HIROYUKI
KUMAMOTO TOSHIO
IGARASHI MOTOSHIGE
YAMAGUCHI KENJI
APPLICANT(s): MITSUBISHI ELECTRIC CORP
APPL. NO.: 2001-059948 [JP 20011059948]
FILED: March 05, 2001 (20010305)

ABSTRACT

PROBLEM TO BE SOLVED: To improve reliability, by forming **resistance elements** having desired shapes on an element **isolating oxide film** and enhancing the precision of a resistance value.

SOLUTION: In this semiconductor device, in which a plurality of the **resistive elements** 4 are formed on the element **isolating oxide film** 2 in a prescribed region formed on the surface of a semiconductor substrate 1, **active regions** 3 are arranged at positions adjacent to the **resistance elements** 4. Thereby the element **isolating oxide film** 2 in the vicinities of the **resistance elements** 4 can be partitioned in necessary regions, and the formation of a recessed part in a central part of the element **isolation oxide film** 2 can be restrained, when the film 2 is **polished** by a **CMP** method, so that the dimensional accuracy of the shapes of the **resistive elements** 4 can be improved.

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35/3,AB/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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03915536

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 04-280636 [JP 4280636 A]
PUBLISHED: October 06, 1992 (19921006)
INVENTOR(s): TANI SATORU
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-043603 [JP 9143603]
FILED: March 08, 1991 (19910308)
JOURNAL: Section: E, Section Number 1322, Volume 17, Number 85, Pg. 86, February 19, 1993 (19930219)

ABSTRACT

PURPOSE: To stabilize the contact, etc., between wirings by a method

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Irina Speckhard

308-6559

wherein the leading-out conductive layer, etc., of *****resistors***** and active **elements** are buried in field **oxide films** so that the field **oxide films** may be flush with the leading-out conductive layers, etc., of *****resistor***** and active *****elements*****

CONSTITUTION: Field **oxide films** 2 are formed to leave *****active***** element *****region***** 4 parts by LOCOS step, etc., on an Si substrate 1 and then the field **oxide films** 2 are etched away to form resistance regions 3. Simultaneously with said steps, the peripheral parts exposing the Si substrate 1 are etched away to be expanded for the formation of the *****active***** element *****region***** 4 parts. Next, the first polycrystalline semiconductor layers 5 are formed on the whole surface of the Si substrate 1 and then the **surface** is **polished** so as to make the polycrystalline semiconductor layer 5 in the resistance regions 3 and the active element regions 4 flush with the field *****oxide***** *****films***** 2. Through these procedures, the surface where active **element**, **resistors** are formed can be flattened thereby enabling the stable contact, etc., between wirings to be made.

35/3,AB/3 (Item 3 from file: 347)
 DIALOG(R)File 347:JAPIO
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01779040
 PRODUCTION OF SEMICONDUCTOR DEVICE

PUB. NO.: 60-257540 [JP 60257540 A]
 PUBLISHED: December 19, 1985 (19851219)
 INVENTOR(s): SAKURAI HIROMI
 APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
 APPL. NO.: 59-115884 [JP 84115884]
 FILED: June 04, 1984 (19840604)
 JOURNAL: Section: E, Section Number 402, Volume 10, Number 125, Pg. 100, May 10, 1986 (19860510)

ABSTRACT

PURPOSE: To provide an **element** having high pressure **resistance**, by a method in which a sputter **oxide film** is formed on the surface of a substrate to have a thickness of 5 μ m or more and is provided in a part thereof with an aperture, which is filled with a semiconductor grown epitaxially, and the upper face of the epitaxially grown **film** is **polished** to be flattened, so that an **active** *****region***** isolated by the sputter *****oxide***** *****film***** is provided.

CONSTITUTION: Boron is implanted in the upper face of a p type Si substrate 1 for forming a channel cut layer 2. Subsequently, a 11 μ m thick sputter SiO(sub 2) film 3a is formed thereon. The sputter SiO(sub 2) film 3a is then provided with an aperture 4, through which arsenic is implanted to form an n(sup +) type buried collector layer 5. After that, Si is caused to epitaxially grow selectively so as to have a thickness of about 12 μ m. The Si *****film***** is then *****polished***** to reduce the thickness to 10 μ m and to flatten the surface. In this manner, an *****active***** *****region***** isolated by the SiO(sub 2) film is obtained. Since the *****active***** *****region***** thus obtained has a thickness as large as 10 μ m, an element having a sufficiently high pressure resistance can be obtained.

37/3,AB/1 (Item 1 from file: 350)
 DIALOG(R)File 350:Derwent WPIX
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013522127

WPI Acc No: 2001-006333/200101

Related WPI Acc No: 2000-136470; 2001-289739; 2002-163024

XRAM Acc No: C01-001377

XRPX Acc No: N01-004510

Capacitor storage node forming method for fabrication of DRAM, involves removing portion of BPSG layer by anisotropic dry etching to form elongated stem-like openings of minimum photolithographic dimension

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: PAREKH K R

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6140172	A	20001031	US 97798251	A	19970211	200101 B
			US 98204749	A	19981202	

Priority Applications (No Type Date): US 97798251 A 19970211; US 98204749 A 19981202

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6140172	A		32	H01L-021/8234	Div ex application US 97798251

Abstract (Basic): US 6140172 A

Abstract (Basic):

NOVELTY - A borophosphosilicate glass (BPSG) layer (34a) is formed on a semiconductor substrate at nodal areas (25a,27a,29a). The portions of BPSG layer masked and unmasked by polysilicon layer, are removed by anisotropic dry etching and subsequent isotropic wet etching to form a tapered elongated stem-like openings having dimensions lesser than minimum photolithographic dimensions.

DETAILED DESCRIPTION - Undoped polysilicon masking layer is patterned on BPSG layer (34a). INDEPENDENT CLAIMS are also included for the following: (i) Capacitor forming method which involves forming a sacrificial silicon **oxide layer** over an etch restriction layer (102) within the tapered elongate stem-like openings. Doped polysilicon pedestals (116b-118b) extending into the BPSG layer, are formed in the openings, after etching the etch restriction layer and BPSG layer (34a). The sacrificial layer is removed to form gap between the lateral surfaces of the pedestals and the BPSG layer. A storage node layer, is formed adjacent the lateral surfaces of the pedestal and a masking layer is formed over the node layer. The unmasked portion of the node layer is removed and the node *****layer***** is *****polished*****. A **dielectric layer** and a cell plate layer are formed adjacent the node layer to form the capacitor; (ii) Bitline construction method which involves forming the stem-like openings underlying the BPSG layer, not extending to the nodal areas and forming another pair of openings extending from the prior set of openings to the nodal areas by removing portion of the BPSG and the sacrificial layers. Gap is formed between the BPSG layer and the pedestals and storage node layer, *****dielectric***** layer and cell plate layer are formed in the gap. Another BPSG layer is formed over the prior BPSG layer and the pedestals. Portion of the secondary BPSG layer in one of the gaps is removed to expose the pedestals and the capacitor layers. The pedestal

and the capacitor layers are partially removed. An electrically conductive bitline plug is formed in electrical connection with the exposed pedestal; (iii) DRAM array construction method which involves forming bitlines over the capacitors formed in the gap between pedestal and the BPSG layer (34a), where the exposed pedestal and the capacitor connected to the bitlines form the DRAM cell; (iv) Monolithic integrated circuit forming method which involves forming capacitor, transistor and **resistive elements** on the semiconductor substrate in which the transistor gate (26a) electrically couples the nodal areas.

USE - For fabrication of DRAM cell used in microprocessor.

ADVANTAGE - The etching of the BPSG layer and the etch restriction layer before pedestal formation, ensures adequate clearance around upper corners of the pedestals for subsequent capacitor formation.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the wafer fragment during DRAM cell construction.

Nodal areas (25a,27a,29a)

Transistor gate (26a)

Borophosphosilicate glass layer (34a)

Etch restriction layer (102)

Doped polysilicon pedestals (116b-118b)

pp; 32 DwgNo 22/22

37/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013087842

WPI Acc No: 2000-259714/200023

XRAM Acc No: C00-079695

XRPX Acc No: N00-193257

Planarization of **oxide film** for manufacturing semiconductor device, involves implanting phosphorus ion using resist **film** as mask before **polishing** process

Patent Assignee: NIPPON STEEL CORP (YAWA)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11340174	A	19991210	JP 98164212	A	19980528	200023 B

Priority Applications (No Type Date): JP 98164212 A 19980528

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 11340174	A	4	H01L-021/304	

Abstract (Basic): JP 11340174 A

NOVELTY - Multiple transistor elements (TR) are formed on a semiconductor substrate (11). An *****oxide***** *****film***** (12) is formed on the substrate. The phosphorus ion is implanted into the *****oxide***** **film** via a resist film (13) which is formed on a recess in

*****oxide***** *****film***** as a mask. Then, the *****oxide***** *****film***** is *****polished*****.

USE - For manufacturing semiconductor device.

ADVANTAGE - Flat **oxide film** is obtained irrespective of its background pattern by uniform **polishing** process, since the **layer insulation** film is not dependent on the roughness and

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fineness of element pattern formed on semiconductor substrate.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of
processes involved in semiconductor device manufacture. (11)
Semiconductor substrate; (12) **Oxide** film; (13) **Resist**
film ; (TR) Transistor ***elements***
Dwg.1/5

37/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010100882

WPI Acc No: 1995-002135/199501

XRAM Acc No: C95-000850

XRFX Acc No: N95-001856

Preparation of magneto-resistance effect type magnetic head - by laminating a
polycrystalline ferrite substrate, an **insulating** layer, a soft
magnetic film, etc., for magnetic disc device

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU .)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 6290424	A	19941018	JP 9373203	A	19930331	199501 B

Priority Applications (No Type Date): JP 9373203 A 19930331

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 6290424	A	4	G11B-005/39	

Abstract (Basic): JP 6290424 A

Method is effected by lamination of a polycrystalline ferrite
substrate, an **insulating** layer of which **surface** is
polished, a soft magnetic **film**, an intermediate layer
having magneto **resistance** effect **element** and
diaferromagnetic film with lead portion at the both ends; an
oxide layer, lower magnetic **layer** with magnetic gap
portion and a Cu coil portion for write, an **insulating** layer and
an upper magnetic layer in that order.

USE/ADVANTAGE - The head is suitable for magnetic disc device. It
has improved reliability, since the films and layers have improved
running life by **polishing surface** of the **insulating**
layer.

Dwg.2/6

37/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009896377

WPI Acc No: 1994-176293/199421

Related WPI Acc No: 1994-316282

XRAM Acc No: C94-080698

XRFX Acc No: N94-138849

Production of multi-value linear resistors for IC using single mask level -
includes using number of trenches of specified lateral dimensions which
are filled with 2 conductive layers of high and low resistivity and a

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09/960,495

dielectric layer and planarised

Patent Assignee: NORTHERN TELECOM LTD (NELE)

Inventor: BOYD J M; ELLUL J P; TAY S P

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5316978	A	19940531	US 9337048	A	19930325	199421 B

Priority Applications (No Type Date): US 9337048 A 19930325

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5316978	A	15	H01L-021/3205	

Abstract (Basic): US 5316978 A

A multi-valued linear resistors for an integrated circuit is obtd. using a single mask level a number of trenches are defined in a substrate. Each *****trench***** has contact regions of a specific lateral dimension and a narrower portion extending between them successive conformal layers of a first dielectric layer, a first conductive layer of high resistivity and a second conductive layer of lower resistivity are provided to fill the *****trench*****. The amount of the second conductive layer which fills the **trench** depends on the width of the *****trench*****. The resulting structure is planarised, pref. by **chemical mechanical polishing** to provide fully planarised topography.

When the first and second conductive layers are provided from layers of undoped and doped polysilicon respectively, the **trench** dimensions control the amount of dopant incorporated in each region of the trench. After annealing to diffuse the dopant, the wider end contact regions are heavily doped to form contact regions, and the intermediate narrow portion of the **trench** is doped to a level dependent on the width of the **trench**, thereby forming a **resistive element** having a **resistivity** inversely dependent on the *****trench***** width.

ADVANTAGE - The method is compatible with CMOS, Bipolar and Bipolar CMOS processes.

Dwg. 6a-c/8

37/3,AB/5 (Item 1 from file: 347)

DIALOG(R) File 347:JAPIO

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05375141

SUPERCONDUCTING ELEMENT AS WELL AS ITS MANUFACTURE AND OPERATING METHOD

PUB. NO.: 08-330641 [JP 8330641 A]

PUBLISHED: December 13, 1996 (19961213)

INVENTOR(s): TARUYA YOSHINOBU

SUGII NOBUYUKI

FUKAZAWA TOKUMI

KABASAWA TAKANORI

HASEGAWA HARUHIRO

TAKAGI KAZUMASA

APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 07-134886 [JP 95134886]

FILED: June 01, 1995 (19950601)

EIC2800

Irina Speckhard

308-6559

ABSTRACT

PURPOSE: To obtain a superconducting element whose circuit constitution and operating system are simplified and which can be operated at high speed by a method wherein a gate voltage which is applied to a gate electrode is used as an input signal as well as a tunnel resistance value and a superconducting current value are controlled.

CONSTITUTION: (100) plane orientations of two strontium titanate single crystals are made to agree, the orientations are displaced by a prescribed angle inside a plane so as to be bonded, a bicrystal single crystal having a grain boundary 2 is cut at the (100) plane orientations, and a substrate 1 for a superconducting element is formed. The central part 3 on the rear of the substrate 1 is chemically **polished**, and a **surface** is formed as a mirror surface. Then, a Ba-K-Bi ***oxide*** thin ***film*** having a tunnel ***insulating*** layer 5 is formed on the surface. Then, a wiring pattern, a source electrode 4, a drain electrode 6, a **resistance element** and the like for the superconducting element are formed on the Ba-K-Bi ***oxide*** thin ***film***. Then, an Au film is formed on the rear of the substrate 1, and a gate electrode 7 is formed. A tunnel resistance value and a current value are controlled by a gate voltage.

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39/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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06570642

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 2000-156420 [JP 2000156420 A]
PUBLISHED: June 06, 2000 (20000606)
INVENTOR(s): MIYAHARA SUSUMU
APPLICANT(s): NEC CORP
APPL. NO.: 10-330691 [JP 98330691]
FILED: November 20, 1998 (19981120)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce a difference between the depths of contact holes which are formed on a ***resistance*** ***element*** and a device.

SOLUTION: A device, such as a transistor, is formed in a silicon substrate 1. An oxide ***film*** 2, a nitride ***film*** 3 and an ***oxide***

film 4 are laminated in order on the substrate 1 formed with the device to form the films 2, 3 and 4. A groove for forming a **resistance element 8** in a prescribed region of the film 4 is formed in the film 4. A nitride film 5 having a film thickness in the extent that the groove is not filled with the film 5 is formed on the film 4 formed with the groove. A polycrystalline silicon film is **polished** using the film 5 as a stopper to form the **resistance element 8** in the prescribed region of the ***film*** 4. An ***oxide*** ***film*** 9

and a BPSG film 10 are laminated on the film 5 formed with the element 8 to form the films 9 and 10 on the film 5, and contact holes 11 are formed on the element 8 and the device to provide a wiring.

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DIALOG(R)File 347:JAPIO
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06412742

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 11-354400 [JP 11354400 A]
PUBLISHED: December 24, 1999 (19991224)
INVENTOR(s): SAINO KANTA
APPLICANT(s): NEC CORP
APPL. NO.: 10-164719 [JP 98164719]
FILED: June 12, 1998 (19980612)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent drop of alignment precision by allowing at least a part of the alignment mark provided on a substrate to protrude above a substrate surface.

SOLUTION: A nitride film 3 is formed on a pad oxide film 2 formed on an Si substrate 1, on which a photo-resist element separation pattern is formed. Then, the nitride film 3 and the pad oxide film 2 are sequentially ion-etched, reactive anisotropically, to expose the Si substrate 1. Then, after the photo-resist is released, the Si substrate 1 is anisotropically etched with the nitride film 3 as a mask to form a groove 4. Then, with the nitride film 3 as a mask, the Si substrate 1 is thermally oxidized to form a thermal oxide film 5 on a side wall and a bottom surface of the groove 4. Then a CVD ***oxide*** ***film*** 6 is deposited to bury the groove 4 appropriately, and CMP is so performed as to expose the nitride film 3 for flattened CVD ***oxide*** ***film*** 6. Then, etching is performed using a mask wherein a photo-resist 7 is patterned, to adjust the height of the upper surface of the CVD ***oxide*** ***film*** 6.

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06356092

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURE

PUB. NO.: 11-297700 [JP 11297700 A]
 PUBLISHED: October 29, 1999 (19991029)
 INVENTOR(s): NOGUCHI JUNJI
 YAMAGUCHI HIDE
 OWADA NOBUO
 APPLICANT(s): HITACHI LTD
 APPL. NO.: 10-104629 [JP 98104629]
 FILED: April 15, 1998 (19980415)

ABSTRACT

PROBLEM TO BE SOLVED: To surely avoid corrosion of metal wirings or metal plugs formed by the COMPONENTS method.

SOLUTION: A light shield layer 20 of e.g. a Cu film is formed above p-type semiconductor regions 4 constituting terminal resistance elements R, at the same time as a step of polishing the Cu film deposited to an upper part of an Si oxide film 21 by the CMP method to form second layer wirings 17-19, and has a wide area enough to cover approximately the entire p-type semiconductor region 4. By placing the light shield layer 20 above the p-type semiconductor region 4, the light incidence on the p-type semiconductor region 4 can be avoided in the step of polishing the Cu film by the CMP method to form the second layer wirings 17-19, and the corrosion of the wirings 17-19 due to a photo current generated by a light incident on the p-n junction is avoided.

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04952834

WIRING FILM AND NONLINEAR RESISTOR ELEMENT AND THIN-FILM TRANSISTOR AND LIQUID-CRYSTAL DISPLAY AND SEMICONDUCTOR DEVICE AND MANUFACTURE OF WIRING FILM AND NONLINEAR RESISTOR ELEMENT AND THIN-FILM TRANSISTOR AND SEMICONDUCTOR DEVICE

PUB. NO.: 07-245434 [JP 7245434 A]
PUBLISHED: September 19, 1995 (19950919)
INVENTOR(s): INOUE TAKASHI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-032428 [JP 9432428]
FILED: March 02, 1994 (19940302)

ABSTRACT

PURPOSE: To manufacture high-quality wiring films without defects with less dispersion of quality by simple processes, by grinding a metal layer and forming an anode ***oxide*** ***film*** on the surface of the metal layer.

CONSTITUTION: A wiring film 12 is composed of elements including Ta being a main component. And the wiring film 12 patterned into a specified shape is electrolytically polished by making the film an anode, and applying voltage between the film and a cathode 10. An electrolytic solution used for the electrolytic polishing on this occasion is an aqueous solution containing 0.5-7% of hydrofluoric acid and 32-38% of hydrochloric acid, and the electrolytic polishing is performed by an impressed voltage 40-60V, and a current density 0.1-0.2A/cm². After that, the substrate 11 is cleaned with pure water and the water is swished off. Then it is dipped in an anode oxidizable electrolytic solution, and an anode oxide film 13 is deposited on the surface of the wiring film 12. As a result of this, it becomes possible to obtain high-quality wiring films having few defects without quality dispersion by simple processes.

39/3,AB/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
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01688848

MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 60-167348 [JP 60167348 A]
PUBLISHED: August 30, 1985 (19850830)
INVENTOR(s): IINO TERUO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-022244 [JP 8422244]
FILED: February 09, 1984 (19840209)
JOURNAL: Section: E, Section Number 371, Volume 10, Number 1, Pg. 128, January 07, 1986 (19860107)

ABSTRACT

PURPOSE: To eliminate the failure of the chips due to crystal defect or the photo masks damaged by such protrusions as mounts and pits formed on the surface of the epitaxial layer and to upgrade the yield of the semiconductor device by a method wherein such elements as transistor, resistor and so forth are formed on the back surface of the semiconductor substrate with the main surface whereon the epitaxial layer

has been formed.

CONSTITUTION: A prescribed part of an **oxide film 2** is selectively removed, N type impurities are diffused and an N type impurity region 4 is formed in such a way that the region 4 holds a constant plane-wise distance to P type impurity regions 3. At this time, P type silicon layers 5 grown on the **oxide film 2** left are turned into polycrystalline silicon layers and P type silicon layers 6 formed on the impurity diffusion regions 3 and 4 are turned into epitaxial layers. P type impurities are diffused up to reach the P type regions 3 from the prescribed parts 8, 8a and 8b on the **polished back surface 7a** of the N type silicon substrate 1. Lastly, P type impurity regions 10 and 10a and N type impurity regions 11 and 11a are formed in order in the back surface 7a of the N type silicon substrate 1, and P type **resistance** layers and such **elements** as N-P-N transistor and so forth are formed.

43/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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6747734 INSPEC Abstract Number: B2000-12-2550F-031
Title: Sheet resistance control in a copper dual damascene integration scheme
Author(s): Allers, K.-H.; Matusiewicz, G.R.
Author Affiliation: Infineon Technol., Hopewell Junction, NY, USA
Conference Title: ULSI Process Integration. Proceedings of the First International Symposium (Electrochemical Society Proceedings Vol.99-18) p.367-75
Editor(s): Claeys, C.L.; Iwai, H.; Bronner, G.; Fair, R.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1999 Country of Publication: USA xiii+386 pp.
ISBN: 1 56677 241 9 Material Identity Number: XX-2000-00269
Conference Title: Proceedings of ULSI Process Integration
Conference Sponsor: Electrochem. Soc
Conference Date: 17-22 Oct. 1999 Conference Location: Honolulu, HI, USA

Language: English
Abstract: The systematic effects on the metal sheet resistance in a copper dual damascene integration scheme using SiO₂/sub 2/ as dielectric were analysed and quantified. The resistivity of copper is 1.9 $\mu\Omega$ cm+or-0.15 $\mu\Omega$ cm, independent of line width and verified under production-like conditions. The dominant effects on sheet resistance for narrow lines <0.5 μ m are a line width dependent ***trench*** depth. For wide lines >1 μ m, the copper CMP process dominates the sheet **resistance-wide** lines in high pattern factor environments being thinner than isolated lines. This behaviour recommends a limitation of the maximum line width and pattern factor in order to achieve an optimum sheet resistance with low variability.
Subfile: B
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43/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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6120526 INSPEC Abstract Number: B1999-02-2550F-016
Title: Fabrication of Cu interconnects of 50 nm linewidth by electron-beam lithography and high-density plasma etching
Author(s): Hsu, Y.; Standaert, T.E.F.M.; Oehrlein, G.S.; Kuan, T.S.; Sayre, E.; Rose, K.; Lee, K.Y.; Rossnagel, S.M.
Author Affiliation: Dept. of Phys., State University of New York, Albany, NY, USA
Journal: Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures) Conference Title: J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct. (USA) vol.16, no.6 p.3344-8
Publisher: AIP for American Vacuum Soc,
Publication Date: Nov.-Dec. 1998 Country of Publication: USA
CODEN: JVTBD9 ISSN: 0734-211X
SICI: 0734-211X(199811/12)16:6L:3344:FILE;1-D
Material Identity Number: C067-1998-007
U.S. Copyright Clearance Center Code: 0734-211X/98/16(6)/3344(5)/\$15.00
Conference Title: 42nd International Conference on Electron, Ion, and

11/14/2003

09/960,495

Photon Beam Technology and Nanofabrication

Conference Date: 26-29 May 1998 Conference Location: Chicago, IL, USA

Language: English

Abstract: The feasibility of building Cu interconnects with a linewidth as small as 50 nm embedded in insulating SiO₂ has been explored using the damascene process. Fine line test structures, designed for evaluating effects of small linewidth on metal line electric resistivity, were written on a poly(methylmethacrylate) resist layer and then transferred to the underlying SiO₂ layer by high-density plasma etching. Using a CHF₃ etching gas and an inductive power of 400 W, we were able to produce 50-nm-wide and 150-nm-deep trenches in SiO₂. These trenches were then filled with a thin (5-10 nm) TaSiN or TaN liner and a thick Cu layer by the ionized physical vapor deposition technique. The field Cu was removed by a **chemical-mechanical polishing** process, leaving narrow damascene Cu in the oxide trenches. Direct current resistance measurements have indicated a **wide** distribution of **resistivity** in these fine lines. The low end of the distribution is close to the effective resistivity of a perfect Cu line. The high values are indicative of severe necking or other imperfections induced during the fabrication process.

Subfile: B

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43/3,AB/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

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5757524 INSPEC Abstract Number: A9801-7475-006, B9801-3220-006

Title: The microstructure and rf performance of YBa/sub 2/Cu/sub 3/O/sub 7-delta / superconducting film for accelerating cavity

Author(s): Wu, B.M.; Lu, J.; Fang, J.G.; Wu, Z.Y.

Author Affiliation: Laboratory of Struct. Anal., University of Sci. & Technol. of China, Hefei, China

Journal: Chinese Journal of Low Temperature Physics vol.19, no.1 p. 39-44

Publisher: Science Press,

Publication Date: Feb. 1997 Country of Publication: China

CODEN: DWXUES ISSN: 1000-3258

SICI: 1000-3258(199702)19:1L:39:MPYS;1-W

Material Identity Number: L877-97002

Language: English

Abstract: For the possible applications of high T_c/oxide superconducting films to rf accelerating cavities the electrophoretic technique was applied to coat YBa/sub 2/Cu/sub 3/O/sub 7-delta / superconductor on a silver technical substrate. The superconducting film and the substrate taken together were machined and *****polished*****. The **surface** resistance of YBa/sub 2/Cu/sub 3/O/sub 7-delta / film at 77 K is 0.6 mW at 500 MHz and 21.88 mW at 35 GHz respectively, significantly lower than that of pure metal. The microstructure of the deposited YBa/sub 2/Cu/sub 3/O/sub 7-delta / film and rf properties of the films including **surface resistance**, **resonant frequency shift**, frequency dependence of R, and high field behavior etc. were studied.

Subfile: A B

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43/3,AB/4 (Item 1 from file: 8)

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09/960,495

DIALOG(R)File 8:EI Compendex(R)
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05197394

E.I. No: EIP99014524119

Title: Extendibility of Cu damascene to 0.1 μm wide interconnections

Author: Hu, C-K.; Lee, K.Y.; Gignac, L.; Rossnagel, S.M.; Uzoh, C.; Chan, K.; Roper, P.; Harper, J.M.E.

Corporate Source: T.J. Watson Research Cent, Yorktown Heights, NY, USA

Conference Title: Proceedings of the 1998 MRS Spring Symposium

Conference Location: San Francisco, CA, USA Conference Date: 19980413-19980416

E.I. Conference Number: 48894

Source: Advanced Interconnects and Contact Materials and Processes for Future Integrated Circuits Materials Research Society Symposium - Proceedings v 514 1998. MRS, Warrendale, PA, USA. p 287-292

Publication Year: 1998

CODEN: MRSPDH ISSN: 0272-9172

Language: English

Abstract: We demonstrate the extendibility of the Cu damascene process to 0.1 μm wide lines. Cu interconnects, 0.1 - 1 μm wide, were fabricated by a damascene process that produced planarized lines and vias, imbedded in insulators. This process was defined by 1) *****trench***** and via formation in blanket dielectrics using e-beam lithography and reactive ion etching, 2) **trench** fill using a series of metal depositions, and 3) *****chemical***** *****mechanical***** *****polishing***** to remove the field metals.

Physical vapor and ionized physical vapor deposition techniques were used to deposit the adhesion/diffusion barrier liner and the Cu seed layer, respectively. The main Cu conductor was deposited by an electroplating method. The width of lines and vias were varied from 0.1 μm to 1 μm while the thicknesses were held constant at 0.45 μm . A near bamboo-like structure was observed in the sub- μm *****wide***** lines. The effective *****resistivity***** of the Cu lines was found to be about 2.3 $\mu\Omega\text{-cm}$ and was independent of width after annealing at 400 degree C. (Author abstract) 11 Refs.

43/3,AB/5 (Item 1 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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07395554 Genuine Article#: 160LU Number of References: 3

Title: Applications of tetramethylammonium hydroxide (TMAH) as a post tungsten **CMP** cleaning mixture (ABSTRACT AVAILABLE)

Author(s): Jolley M

Journal: SOLID STATE PHENOMENA, 1999, V65-6, P105-108

ISSN: 1012-0394 Publication date: 19990000

Publisher: TRANS TECH-SCITEC PUBLICATIONS LTD, BRANDRAIN 6, CH-8707 UETIKON A.S., SWITZERLAND

Language: English Document Type: ARTICLE

Abstract: Modern integrated circuit manufacturing relies on **chemical mechanical polishing(CMP)** to smooth the dielectric layers that are used between conducting metal layers as electrical insulation. It (*****CMP*****) is also used in a damascene type process to fabricate metal plugs that serve as electrical connectors between metal layers. The usual plug is formed out of tungsten with a liner layer composed of titanium and titanium nitride. The typical polishing slurry

for the tungsten and glue layer is a mixture of aluminum oxide abrasive and a chemical oxidizer. The most common oxidizer is ferric nitrate. Most polishing sequences do a touch up polish with colloidal silica after the tungsten polish step. This removes a thin ***layer*** of oxide and is thought to remove scratches and damage done to the oxide ***surface*** during the tungsten ***polish*** step.

After the tungsten CMP polish is completed the wafer has three distinct surfaces that need to be cleaned. The majority of the product side surface is oxide, while the remainder is the freshly ***polished*** ***surface*** of the tungsten plug. Both surfaces are contaminated with residual slurry and need to be cleaned. In addition the backside of the wafer also needs to be cleaned. The process of record for this cleaning step has historically been with contact cleaning using PVA brushes. Recently several authors have suggested non-contact cleaning techniques based alkaline solutions' or dilute mixtures of HF with added anionic surfactants(2).

Alkaline or high pH solutions remove particles via a slight etching of the surface. As the particles are undercut by the etching they are lifted off the surface. These solutions etch both the ***oxide*** films and the exposed metal films on the order of Angstroms per minute. In most cases the electrostatic forces are such that the particle does not re-adhere to the wafer surface being cleaned. The two most likely candidates for this type of cleaning are dilute solutions based on either ammonium hydroxide or tetramethylammonium hydroxide (TMAH). Both are commonly used in semiconductor manufacturing. Ammonium hydroxide is a component in pre-diffusion wafer cleaning schemes and TMAH is ***widely*** used as a ***resist*** developer.

TMAH is a strong base, while ammonium hydroxide is a weak base. This means that solutions based on TMAH can be of higher pH than solutions based on ammonium hydroxide. Another difference is in etch rate on ***oxide*** ***films***. At comparable temperature's and concentration's TMAH based solution's etch rates are almost an order of magnitude slower than ammonium hydroxide based solutions. This is probably due to the large size of the TMAH cation as compared to the ammonium hydroxide cation. This may be an advantage when cleaning films doped with phosphorus or boron. Another potential advantage of TMAH based solutions may be improved surface metal removal because of their increased pH(3).

This paper discusses a series of experiments performed using TMAH as a cleaning chemistry after a tungsten ***CMP*** polish. All work was done on 150 mm wafers. Prior to ***polish*** the ***film*** stack consisted of a TEOS base layer with a Ti/TiN/Tungsten stack deposited on top of the TEOS. The wafers were given a typical two step polish. The first step used an alumina based slurry to remove the metal's stack and a second polish with a silica based slurry to remove the scratches induced during the metal polish. After polish the wafers were cleaned in a Semitool spray acid tool. The cleaning chemistry was based on TMAH solutions at 80 degrees C applied for 10 to 20 minutes. After the polish and the clean in the Semitool particle counts were taken on a Tencor 6420 particle counter at a threshold of 0.2 micron. The effect of added surfactant, amount of removal during the clean step and the normality of the TMAH solution will be discussed.

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43/3,AB/6 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015534042

WPI Acc No: 2003-596192/200356

XRAM Acc No: C03-161305

XRFX Acc No: N03-475107

Formation of short channel metal oxide semiconductor transistor involves implanting first ions underlying **oxide spacers** to form source/drain extensions, and implanting second ions adjacent gate electrode

Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)

Inventor: CHAN L; CHONG Y F

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6566215	B1	20030520	US 2002163687	A	20020606	200356 B

Priority Applications (No Type Date): US 2002163687 A 20020606

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6566215	B1	11		H01L-021/336	

Abstract (Basic): US 6566215 B1

Abstract (Basic):

NOVELTY - The formation of a short channel metal oxide semiconductor (MOS) transistor comprises filing a second opening between the **spacers** with polysilicon **layers**, and the *****oxide***** *****spacers***** are removed. The first ions are implanted into the substrate underlying the **oxide spacers** to form source/drain extensions. The second ions are implanted to form source/drain regions within the substrate adjacent the gate electrode.

DETAILED DESCRIPTION - The formation of a short channel MOS transistor comprises forming a hard mask stack over a substrate (10), a first opening, and **oxide spacers** on sidewalls, in sequence over a substrate. The second opening between spacers is filled with polysilicon **layers**, and the **oxide spacers** are removed. The first ions are implanted into the substrate underlying the *****oxide***** *****spacers***** to form source/drain extensions (36). The polysilicon layer is removed while leaving the first opening and exposing the substrate in a channel region. A gate dielectric layer (40) is formed over the channel region. The first opening is filled with gate electrode material and the gate electrode material is polished back to form a gate electrode (44). The hard mask stack is removed using the gate electrode as a mask. The second ions are implanted to form source/drain regions within the substrate to the gate electrode to complete formation of the short channel MOS transistor in the production of the integrated circuit device.

USE - Used for forming a short channel MOS transistor.

ADVANTAGE - The process utilizes existing lithographic technologies and mask sets. It provides a transistor having an increased gate *****width***** and reduced gate *****resistance*****.

DESCRIPTION OF DRAWING(S) - The drawings show cross-sectional views of last steps in the process.

Substrate (10)

Source/drain extensions (36)

Gate dielectric layer (40)

11/14/2003

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Gate electrode (44)

pp; 11 DwgNo 7, 9, 11, 13/14

43/3,AB/7 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009880706

WPI Acc No: 1994-160620/199420

XRAM Acc No: C94-073571

XRPX Acc No: N94-126368

Trench isolation planarisation for IC fabrication - uses hard mask
over surface with **resist** in **wide** trenches and etches back to
leave falt dielectric which is polished to remove peaks

Patent Assignee: DIGITAL EQUIP CORP (DIGI)

Inventor: GRULA G J; WANG C

Number of Countries: 004 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 597603	A2	19940518	EP 93308495	A	19931025	199420 B

Priority Applications (No Type Date): US 92975871 A 19921113

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 597603	A2	E	12	H01L-021/76	

Designated States (Regional): DE FR GB IT

Abstract (Basic): EP 597603 A

The process for planarising an isolation **trench** in semiconductor fabrication includes the use of a hard maask. The semiconductor has wide (20), medium (22) and narrow (24) trenches separating area mesas (33) with devices (34). A layer of dielectric (36) such as TEOS is deposited on the semiconductor and substantially fills the trenches.

A hard mask (38) is formed over the dielectric and conventional filler resist can be used as an aid on wide trenches. The hard film and the dielectric layers are then etched back and the **surface** can be

polished to remove peaks and depressions. ADVANTAGE - Avoids the formation of depressions in trenches allowing easier planarisation for forming conductors.

Dwg.6/15

43/3,AB/8 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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06622802

PRODUCTION OF SEMICONDUCTOR DEVICE

PUB. NO.: 2000-208613 [JP 2000208613 A]

PUBLISHED: July 28, 2000 (20000728)

INVENTOR(s): YAMAZAKI TAKESHI

APPLICANT(s): SONY CORP

APPL. NO.: 11-010593 [JP 9910593]

FILED: January 19, 1999 (19990119)

EIC2800

Irina Speckhard

308-6559

ABSTRACT

PROBLEM TO BE SOLVED: To prevent a groove near the terminal edge part thereof from being dropped rather than the upper surface of a substrate at the upper part of a **trench** element isolating region and to form the groove of width narrower than opening **width** formable in a *****resist***** pattern.

SOLUTION: An opening 3a is formed on a pad **oxide film** 2 and an SiN film 3 on an Si substrate 1. After a sidewall is formed on the inner peripheral surface of the opening 3a, a groove 6 is formed on the Si substrate 1 with the SiN film 3 and the sidewall as a mask. After the side wall is removed, a thermal **oxide film** 7 is formed on the exposed surface of the Si substrate 1. After an embedded *****oxide***** film 8 is formed by embedding into the groove 6 and the opening 3a through high density plasma chemical vapor deposition(CVD), the embedded **oxide film** 8 on the SiN film 3 is removed and flattening is performed by *****chemical***** - *****mechanical***** *****polishing***** (*****CMP*****). A sacrificial **oxide film** is formed by removing the SiN film 3 and, after the sacrificial **oxide film** is removed, a gate *****oxide***** *****film***** is formed. Thus, the *****trench***** element isolating region is formed.

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-14nov03 10:31:23 User267149 Session D1099.1

SYSTEM:OS - DIALOG OneSearch

File 2:INSPEC 1969-2003/Nov W1

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*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.

File 6:NTIS 1964-2003/Nov W2

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File 8:Ei Compendex(R) 1970-2003/Nov W1

(c) 2003 Elsevier Eng. Info. Inc.

File 34:SciSearch(R) Cited Ref Sci 1990-2003/Nov W2

(c) 2003 Inst for Sci Info

File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec

(c) 1998 Inst for Sci Info

File 35:Dissertation Abs Online 1861-2003/Oct

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File 65:Inside Conferences 1993-2003/Nov W2

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File 94:JICST-EPlus 1985-2003/Nov W2

(c) 2003 Japan Science and Tech Corp(JST)

File 99:Wilson Appl. Sci & Tech Abs 1983-2003/Oct

(c) 2003 The HW Wilson Co.

File 144:Pascal 1973-2003/Nov W1

(c) 2003 INIST/CNRS

File 305:Analytical Abstracts 1980-2003/Oct W3

(c) 2003 Royal Soc Chemistry

*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.

File 315:ChemEng & Biotec Abs 1970-2003/Oct

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File 350:Derwent WPIX 1963-2003/UD,UM &UP=200373

(c) 2003 Thomson Derwent

File 347:JAPIO Oct 1976-2003/Jul(Updated 031105)

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*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.

File 344:Chinese Patents Abs Aug 1985-2003/Apr

(c) 2003 European Patent Office

File 371:French Patents 1961-2002/BOPI 200209

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*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	79	AU=(AMISHIRO, H? OR AMISHIRO H?)
S2	1345	AU=(KUMAMOTO, T? OR KUMAMOTO T?)
S3	6765	AU=(IGARASHI, M? OR IGARASHI M?)
S4	32655	AU=(YAMAGUCHI, K? OR YAMAGUCHI K?)
S5	2	S1 AND S2
S6	2	RD (unique items)
S7	2	S2 AND S3
S8	0	S7 NOT S5
S9	4	S2 AND S4
S10	3	RD (unique items)
S11	1	S10 NOT S5
S12	40795	S1:S4
S13	44	S12 AND (RESIST??????(3N)(PASSIV????? OR ELEMENT? ?))
S14	42	S13 AND ((SHIFT??? OR WIDTH OR WIDE??? OR DIMENSION? ? OR - ELEMENT? ?)(3N)RESIST??????)
S15	2	S14 AND (CMP OR CHEMICAL()MECHANICAL()POLISHING)
S16	2	RD (unique items)
S17	0	S16 NOT S3
S18	0	S16 NOT S5
S19	0	S14 AND (TRENCH? ? OR STI OR SHALLOW()TRENCH()ISOLATION)
S20	0	S14 AND ((PREDETERMIN?????? OR PRE()DETERMIN????? OR SET OR DETERMIN?????)(3N)(WIDTH OR WIDE??? OR LENGTH OR LONG????))
S21	42	RD S14 (unique items)
S22	2	S21 AND ACTIV??????(3N)REGION? ?
S23	2	RD (unique items)
S24	0	S23 NOT S5
S25	2	S21 AND (INSULAT???????? OR DIELECTR??????)
S26	1	S25 NOT S5
S27	40	S21 NOT S25

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6/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014910805

WPI Acc No: 2002-731511/200279

XRPX Acc No: N02-576672

Semiconductor device for analog circuit, has resistor elements formed on insulating oxide film and active regions in contiguous with resistor element

Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ); MITSUBISHI DENKI KK (MITQ)

Inventor: AMISHIRO H; IGARASHI M; KUMAMOTO T; YAMAGUCHI K

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020123202	A1	20020905	US 2001960495	A	20010924	200279 B
JP 2002261244	A	20020913	JP 200159948	A	20010305	200279

Priority Applications (No Type Date): JP 200159948 A 20010305

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
-----------	------	-----	----	----------	--------------

US 20020123202	A1		19	H01L-021/20	
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JP 2002261244	A		13	H01L-027/04	
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Abstract (Basic): US 20020123202 A1

Abstract (Basic):

NOVELTY - Several resistor elements (4) are formed using a MOS transistor gate layer on an insulating oxide film. Several active regions (3) are formed in contiguous with each resistor element cross-wire on both sides. The width of the oxide film is defined by an amount of shift in resistance value of the resistor elements.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for semiconductor device manufacturing method.

USE - Semiconductor device for analog circuit.

ADVANTAGE - Allows the oxide film to be divided into suitable strips, forestalling a concave formation at the center of the film upon polishing of the film by CMP, thereby enhancing dimensional accuracy of the resistor elements upon fabrication. By presetting width of the oxide film, it is possible for the resistor elements to constitute semiconductor devices whose reliability is high enough to meet high precision requirements.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of the semiconductor device.

Active regions (3)

Resistor elements (4)

pp; 19 DwgNo 1A/14

6/3,AB/2 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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07392743

SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

PUB. NO.: 2002-261244 [JP 2002261244 A]

PUBLISHED: September 13, 2002 (20020913)

EIC2800

Irina Speckhard

308-6559

11/14/2003

09/960,495

INVENTOR(s): AMISHIRO HIROYUKI
KUMAMOTO TOSHIO
IGARASHI MOTOSHIGE
YAMAGUCHI KENJI
APPLICANT(s): MITSUBISHI ELECTRIC CORP
APPL. NO.: 2001-059948 [JP 20011059948]
FILED: March 05, 2001 (20010305)

ABSTRACT

PROBLEM TO BE SOLVED: To improve reliability, by forming resistance elements having desired shapes on an element isolating oxide film and enhancing the precision of a resistance value.

SOLUTION: In this semiconductor device, in which a plurality of the resistive elements 4 are formed on the element isolating oxide film 2 in a prescribed region formed on the surface of a semiconductor substrate 1, active regions 3 are arranged at positions adjacent to the resistance elements 4. Thereby the element isolating oxide film 2 in the vicinities of the resistance elements 4 can be partitioned in necessary regions, and the formation of a recessed part in a central part of the element isolation oxide film 2 can be restrained, when the film 2 is polished by a CMP method, so that the dimensional accuracy of the shapes of the resistive elements 4 can be improved.

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11/3,AB/1 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2003 Inst for Sci Info. All rts. reserv.

09550626 Genuine Article#: 418HG Number of References: 29
Title: Synthetic studies on kinamycin antibiotics: elaboration of a highly
oxygenated D ring (ABSTRACT AVAILABLE)
Author(s): **Kumamoto T**; Tabe N; **Yamaguchi K**; Yagishita H; Iwasa
H; Ishikawa T (REPRINT)
Corporate Source: Chiba Univ, Fac Pharmaceut Sci, 1-33 Yayoi/Chiba
2638522//Japan/ (REPRINT); Chiba Univ, Fac Pharmaceut Sci, Chiba
2638522//Japan/; Chiba Univ, Ctr Chem Anal, Chiba 2638522//Japan/
Journal: TETRAHEDRON, 2001, V57, N14 (APR 2), P2717-2728
ISSN: 0040-4020 Publication date: 20010402
Publisher: PERGAMON-ELSEVIER SCIENCE LTD, THE BOULEVARD, LANGFORD LANE,
KIDLINGTON, OXFORD OX5 1GB, ENGLAND
Language: English Document Type: ARTICLE
Abstract: The synthesis of the model compound of kinamycin antibiotics,
which possesses correct relative configurations at C1-C4 on the D ring,
is reported in detail. The key steps involved a Diels-Alder reaction of
indenone (12) and a Danishefsky-type diene (13), and stereoselective
construction of a tetraoxygenated D ring. (C) 2001 Elsevier Science
Ltd. All rights reserved.

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26/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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00671863
CORONA CHARGER

PUB. NO.: 55-159463 [JP 55159463 A]
PUBLISHED: December 11, 1980 (19801211)
INVENTOR(s): HIRANUMA SUSUMU
YAMAGUCHI KENICHI
APPLICANT(s): FUJI XEROX CO LTD [359761] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 54-066065 [JP 7966065]
FILED: May 30, 1979 (19790530)
JOURNAL: Section: P, Section No. 52, Vol. 05, No. 38, Pg. 9, March 12,
1981 (19810312)

ABSTRACT

PURPOSE: To prevent uneven charging without any change in surface potential despite the occurrence of abnormal discharge of the surface to be charged and evenly charge the surface to be charged by using variable impedances.

CONSTITUTION: A Corotron wire 5 which becomes a corona discharge electrode is stretched between a pair of side walls 4, 4 of a shield case 1 of box form having an opening 1a in opposition to the surface 12a to be charged, whereby a charger A is constituted. The bottom wall 2 of the said corona discharge electrode 5 is buried with conductive plate electrodes 6 in its axial direction and the respective electrodes 6 are grounded respectively by way of the variable impedance elements 13 consisting of ***resistance*** ***elements*** 7 and constant voltage elements 8. As the current $i(\text{sub } 0)$ flowing in the Corotron wire 5 increases, the current $i(\text{sub } 2)$ (the current flowing to the earth through the impedance 22 of the air insulation layer between the Corotron wire 5 and bottom wall 2) also increases but the impedance of the variable impedance elements 12 changes and the current flowing in the surface to be charged does not change, hence, the surface potential of the surface 12a to be charged does not change.

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27/3,AB/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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04947130 JICST ACCESSION NUMBER: 01A0752944 FILE SEGMENT: JICST-E
Shear Behavior of Wooden Brace and Panel Elements as Lateral
Resistant Structure.

YAMAGUCHI K (1); MAKITANI E (1); KAJIZUKA M (1); YOSHIDA T (2);
BARRETT J D (3)

(1) Kanto Gakuin Univ.; (2) Kaneshin Co.; (3) Univ. British Columbia, Can
Kanto Gakuin Daigaku Kogaku Sogo Kenkyu Shoho(Bulletin of Institute of
Science and Technology. Kanto Gakuin University), 2001, NO.29,
PAGE.37-42, FIG.11, TBL.3, REF.3

JOURNAL NUMBER: G0426BAB ISSN NO: 0387-2556
UNIVERSAL DECIMAL CLASSIFICATION: 624.011.1 699.841/.842
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: The shear behaviors of a wall structure with diagonal wood
bracing and wood panels (sheathing) were studied. The principal
structural components of the wall were Canadian Hemlock (Canada Tsuga)
and Japanese cedar (Sugi). The study shows that the wall structures
made with Canadian Hemlock posses an excellent and superior shear
characteristics. The test results from these studies also allowed the
calculation of Shear Wall Multiplier Factors used for shear design of
wooden structures in Japan. (author abst.)

27/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012581437
WPI Acc No: 1999-387544/199933
XRPX Acc No: N99-290408

Ceramic heater to be used in semiconductors-producing apparatuses,
etching apparatuses etc.

Patent Assignee: NGK INSULATORS LTD (NIGA); NIPPON GAISHI KK (NIGA)

Inventor: TSURUTA H; USHIKOSHI R; YAMAGUCHI K

Number of Countries: 029 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 929204	A2	19990714	EP 99300119	A	19990107	199933 B
JP 11204238	A	19990730	JP 982306	A	19980108	199941
KR 99066885	A	19990816	KR 9860140	A	19981229	200045
US 6225606	B1	20010501	US 98222223	A	19981229	200126
KR 281954	B	20010215	KR 9860140	A	19981229	200212
TW 518906	A	20030121	TW 98119602	A	19981125	200356

Priority Applications (No Type Date): JP 982306 A 19980108

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 929204	A2	E	15	H05B-003/14	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
LI LT LU LV MC MK NL PT RO SE SI

JP 11204238	A	8	H05B-003/20
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Irina Speckhard

308-6559

11/14/2003

09/960,495

KR 99066885 A H05B-003/14
US 6225606 B1 H05B-003/68
KR 281954 B H05B-003/14 Previous Publ. patent KR 99066885
TW 518906 A H05B-003/00

Abstract (Basic): EP 929204 A2

Abstract (Basic):

NOVELTY - Heater has ceramic substrate with heating surface and **resistance** heating **element** buried inside the substrate A part of the **resistance** heating **element** is constituted by a conductive network member. The ceramic material constituting the ceramic substrate is filled in meshes of the network member. The **resistance** heating **element** has the network member and metallic bulk body integrated with a slender band shaped network member.

USE - For providing a ceramic heater for se in various semiconductor producing apparatuses, etching apparatuses, etc.

ADVANTAGE - Makes it possible to decrease the thickness of the ceramic substrate and provide a high durability on the receipt of heat cycles between high temperature range and room temperature.

DESCRIPTION OF DRAWING(S) - The drawing shows a perspective view of the ceramic heater.

pp; 15 DwgNo 2a/7

27/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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007195091

WPI Acc No: 1987-192100/198727

XRFX Acc No: N87-143821

Electrophotographic light-sensitive element with amorphous C overlayer - has surface protective layer as outermost layer of **element**, to impart **resistance** to environmental conditions

Patent Assignee: FUJI ELECTRIC MFG CO LTD (FJIE)

Inventor: AIZAWA K; HARA K; KAZAMA T; LIJIMA T; YAMAGUCHI K

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4675265	A	19870623	US 86844003	A	19860325	198727 B

Priority Applications (No Type Date): JP 8664565 A 19860328; JP 8561165 A 19850326; JP 8564566 A 19850328; JP 8592785 A 19850430

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 4675265	A	15		

Abstract (Basic): US 4675265 A

The electrophotographic light-sensitive element comprises a conductive support having provided in it sequence: a photoconductive layer comprising amorphous silicon and a surface protective layer comprising hydrogenated amorphous carbon. The concentration of hydrogen atoms in the surface protective layer is from 1 atom percent to 60 atom percent.

The amorphous carbon is mainly bonded in a four-coordinate diamond structure such that the surface protective layer is chemically resistant and has good mechanical strength, and the surface protective

layer has a thickness sufficient to provide humidity resistance but not so great as to result in a significant loss of sensitivity.

ADVANTAGE - Excellent durability, printability and resistance to moisture.

1/9

27/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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004755982

WPI Acc No: 1986-259323/198640

XRPX Acc No: N86-193868

Potentiometer with resistor and collector on base - has housing protrusion on each side surfaces, with depressions between protrusions and corner extensions

Patent Assignee: COPAL CO LTD (COPB); COPAL ELECTRONICS CO LTD (COPB)

Inventor: HORIE T; IGARASHI M; OKAZAKI A

Number of Countries: 003 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 3609655	A	19860925	DE 3609655	A	19860321	198640 B
JP 61216404	A	19860926	JP 8557863	A	19850322	198645
JP 61216405	A	19860926	JP 8557864	A	19850322	198645
JP 61216407	A	19860926	JP 8557868	A	19850322	198645
US 4712084	A	19871208	US 86841455	A	19860319	198751
DE 3609655	C2	19930107	DE 3609655	A	19860321	199301

Priority Applications (No Type Date): JP 8557868 A 19850322; JP 8557863 A 19850322; JP 8557864 A 19850322

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3609655	A		16		
DE 3609655	C2		11	H01C-001/022	

Abstract (Basic): DE 3609655 C

The potentiometer rotor comprises a contact in movable contact with the ***resistance*** and conductive ***elements***. Its housing (24) has a protrusion (32) on either side surface, and depressions (31,33) between the protrusions and corner extensions (28,30). An outer sleeve (2) has two bent long shanks (8) with recesses (10) and two curved walls (17,19), orthogonal to the long shanks.

The sleeve is inserted on the housing so that both long shanks are pressed downwards for snap-connection in the housing depressions, until the protrusions at the housing sides lock into the recesses of the sleeve in a sliding manner. A slider is arranged in a recess and its end is held by a retainer, integral with the rotor. The recess three sides are surrounded by a narrow, bent strip with two front walls.

ADVANTAGE - Miniature construction of flat configuration. (16pp Dwg.No.12/12)

Abstract (Equivalent): DE 3609655 C

A potentiometer includes a base plate on which a **resistive element**, conductive **elements** and a collector element are arranged. A rotor (42) has a slide which engages the ***resistive*** *****element*****. The rotor and base plate are contained in a housing.

The housing has recesses in two opposing side walls in which a projection (32) is arranged, and corner projections (28,30). An outer

sleeve (2) covers an assembly opening of the young and has a through aperture (6) for the rotor. The sleeve has two bent legs corresp. to the dimensions of the recesses with cut-out portions corresp. to the dimensions of the projections. It also has two shorter legs (17,19) at right angles to the long legs. When assembled the cut outs engage with the projections.

ADVANTAGE - Small construction and components are securely fixed in housing. (Dwg.4/12

Abstract (Equivalent): US 4712084 A

The potentiometer has a case, a housing, a base and a rotor rotatably arranged in the chamber of housing. The housing is provided with a pair of projections on both side walls of it and two pair of corner projections at four corners of it respectively while the case has a pair of bent long legs in which holes are defined to receive the side wall projections of the housing and a pair of bent short walls are arranged to cover the top of the housing. The case is pushed down upon the housing with the pair of bent long legs of it are slid down into vertical grooves arranged between the corner projections of the housing until the side wall projections of the housing are slidingly snapped into the holes of the case.

Two end walls of an arcuate portion of a narrow strip are arranged on the surface of the rotor and abut alternatively against two vertical walls of a rectangular strip arranged inside the housing hole and located adjacent a collector element of the base, whenever the rotor rotates in a clockwise or counter-clockwise direction.

ADVANTAGE - Case and housing are assembled in one operation. (9pp)s

27/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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07490257
MAGNETIC MEMORY DEVICE

PUB. NO.: 2002-358775 [JP 2002358775 A]
PUBLISHED: December 13, 2002 (20021213)
INVENTOR(s): IGARASHI MINORU
APPLICANT(s): SONY CORP
APPL. NO.: 2001-163957 [JP 20011163957]
FILED: May 31, 2001 (20010531)

ABSTRACT

PROBLEM TO BE SOLVED: To realize low power consumption, high speed writing, and stable operation in a magnetic memory device represented by a MRAM.

SOLUTION: In the magnetic memory device, which is provided with a magneto **resistive** storage **element** 1, a first write line 2 inducing a magnetic field in the direction of easy magnetizing axis and a second write line 3 inducing a magnetic field in the direction of hard magnetizing axis, and reverses a magnetizing direction of the storage element 1 by a current magnetic field generated by them, the applying timing of a current pulse is controlled so that a current pulse holding time tBL in the first write line 2, a holding time tWL in the second write line 3, and time difference thold between them satisfy the relation of $tBL = tWL + thold$ (thold>0).

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substrate 1, active regions 3 are arranged at positions adjacent to the
resistance ***elements*** 4. Thereby the element isolating oxide film
2 in the vicinities of the **resistance elements** 4 can be
partitioned in necessary regions, and the formation of a recessed part in a
central part of the element isolation oxide film 2 can be restrained, when
the film 2 is polished by a CMP method, so that the dimensional accuracy of
the shapes of the ***resistive*** ***elements*** 4 can be improved.

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27/3,AB/8 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
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07079656
RESISTANCE VALUE DETECTING CIRCUIT

PUB. NO.: 2001-307303 [JP 2001307303 A]
PUBLISHED: November 02, 2001 (20011102)
INVENTOR(s): SAITO HIROSHI
YAMAGUCHI KOJI
WADA SATOSHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD
APPL. NO.: 2000-120800 [JP 2000120800]
FILED: April 21, 2000 (20000421)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a resistance value detecting circuit
having a satisfied PSRR(power supply ripple removal ratio) in such a degree
that the noise entered from the power supply is appeared on a signal output
terminal.

SOLUTION: The resistance value detecting circuit is constituted in such a
manner that resistors R11, R12 are inserted to the bases of transistors
Q11, Q12 for applying currents to a magneto-**resistance element**
RMR1 of a current mirror circuit composed of a constant current source I11,
transistors Q11, Q21, Q31, Q41 and Q12, Q22, Q32, Q42, and further,
capacitors C11, C12 re connected to the bases, other ends of which are
connected to the emitters. By this constitution, potentials between the
bases-emitters of the transistors Q11, Q12 are stabilized by the capacitors
C11, C12 and the resistors R11, R12, and the change of collector currents
is reduced, then the PSRR(Power supply ripple removal ratio) is improved in
the degree such that the noise entered from the power supply is appeared on
the signal output terminal.

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27/3,AB/9 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
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06945189
STEEL EXCELLENT IN COASTAL WEATHER RESISTANCE AND PRODUCING METHOD THEREFOR

PUB. NO.: 2001-172741 [JP 2001172741 A]
PUBLISHED: June 26, 2001 (20010626)

11/14/2003

09/960,495

INVENTOR(s): YAMAGUCHI KIMIHARU
KISHIMOTO YASUO
YAMANE YASUYOSHI
APPLICANT(s): KAWASAKI STEEL CORP
APPL. NO.: 11-358153 [JP 99358153]
FILED: December 16, 1999 (19991216)

ABSTRACT

PROBLEM TO BE SOLVED: To produce weather resistant steel excellent in weather resistance in a coastal zone without requiring coating, surface treatment or the like and furthermore excellent in toughness and weldability.

SOLUTION: In this steel in which a surface layer part and an internal layer part have different compositions, 0.001 to 0.03% C and 0.0003 to 0.005% B are contained, the surface layer part has a composition containing 0.003 to 0.030% P and 1.0 to 6.0% Ni, and also, the internal layer part has a composition containing $\leq 0.030\%$ P and Ni of $\leq 3.0\%$ also below the content of Ni in the surface layer part. Preferably, the thickness of the surface layer part is controlled to ≥ 0.1 mm from the surface of the steel, and the volume ratio of the internal layer part is controlled to $\geq 70\%$ of the whole of the steel. It is preferable that molten steel is poured into a continuous casting mold provided with a d.c. magnetic field zone by using an immersion nozzle and is subjected to continuous casting while an alloy additive containing weather **resistance** improving **elements** such as Ni is added to a molten steel pool located on the part upper than the d.c. magnetic field zone so as to prepare the prescribed surface layer part composition and is made into a slab in which the compositions of the surface layer part and the internal layer part are different.

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27/3,AB/10 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO
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06945188

STEEL EXCELLENT IN COASTAL WEATHER RESISTANCE AND PRODUCING METHOD THEREFOR

PUB. NO.: 2001-172740 [JP 2001172740 A]
PUBLISHED: June 26, 2001 (20010626)
INVENTOR(s): YAMAGUCHI KIMIHARU
KISHIMOTO YASUO
YAMANE YASUYOSHI
APPLICANT(s): KAWASAKI STEEL CORP
APPL. NO.: 11-358152 [JP 99358152]
FILED: December 16, 1999 (19991216)

ABSTRACT

PROBLEM TO BE SOLVED: To produce weather resistant steel excellent in weather resistance in a coastal zone without requiring coating, surface treatment or the like and moreover excellent in toughness and weldability.

SOLUTION: In this steel in which a surface layer part and an internal layer part have different compositions, 0.001 to 0.03% C and 0.0003 to 0.005% B are contained, the surface layer part has a composition containing 0.05 to

0.5% P and 1.0 to 6.0% Ni, and also, the internal layer part has a composition containing $\leq 0.03\%$ P and $\leq 3.0\%$ Ni. Preferably, the thickness of the surface layer part is controlled to ≥ 0.1 mm from the surface of the steel, and the volume ratio of the internal layer part is controlled to $\geq 70\%$ of the whole of the steel. It is preferable that molten steel having the internal layer part composition is poured into a continuous casting mold provided with a direct current magnetic field zone by using an immersion nozzle and is subjected to continuous casting while an alloy additive containing weather **resistance** improving **elements** such as P and Ni is added to a molten steel pool located on the part upper than a d.c. magnetic field zone to form into a slab in which the compositions of the surface layer part and the internal layer part are different.

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27/3, AB/11 (Item 7 from file: 347)
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06185520
 SEMICONDUCTOR CIRCUIT

PUB. NO.: 11-127070 [JP 11127070 A]
 PUBLISHED: May 11, 1999 (19990511)
 INVENTOR(s): NANBU HIROAKI
 HONMA NORIYUKI
 KANETANI KAZUO
 YAMAZAKI SU
 OHATA KENICHI
 ARAKAWA FUMIHIKO
 KUSUNOKI TAKESHI
 HIGETA KEIICHI
 NISHIYAMA MASAHIKO
YAMAGUCHI KUNIIHIKO
 APPLICANT(s): HITACHI LTD
 HITACHI DEVICE ENG CO LTD
 HITACHI ULSI SYSTEMS CO LTD
 APPL. NO.: 09-290716 [JP 97290716]
 FILED: October 23, 1997 (19971023)

ABSTRACT

PROBLEM TO BE SOLVED: To shorten the charging and discharging time of an output signal line and a cycle time by obtaining a discharging circuit which can make cycles fast by supplying the output current signal of a voltage-current converting means to a **resistance element** or load *****element*****.

SOLUTION: The voltage-current converting means VIC1 is provided which converts the voltage of an input signal. IN11 or IN12 or the output signal of a logic gate LG1 receiving the input signal and the output current signal of this voltage-current converting means VIC1 is supplied to the *****resistance***** *****element***** or load *****element***** RB1. Then the base potential of a npn type bipolar transistor QDC1 for discharging is controlled with the output current signal of the voltage-current converting means VIC1. To actualize both charging and discharging, the QDC1, **resistance element** RB1, voltage-current converting means

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VIC1, and a common current source IDC are used for the npn type bipolar transistor, thereby actualizing fast discharging.

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27/3,AB/12 (Item 8 from file: 347)
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05692643
RESISTANCE NETWORK, REFERENCE VOLTAGE GENERATION CIRCUIT USING THE
RESISTANCE NETWORK AND ANALOG-TO-DIGITAL CONVERTER USING THE NETWORK AND
CIRCUIT

PUB. NO.: 09-307443 [JP 9307443 A]
PUBLISHED: November 28, 1997 (19971128)
INVENTOR(s): OKUDA TAKASHI
ITO MASAO
KUMAMOTO TOSHIO
TSUNASHIRO HIROYUKI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 08-096397 [JP 9696397]
FILED: April 18, 1996 (19960418)

ABSTRACT

PROBLEM TO BE SOLVED: To improve the accuracy of resistance value of a resistance network which is used to an A/D converter for generation of the reference voltage.

SOLUTION: The dummy blocks 10 and 11 are placed at both sides of an arrangement area of blocks B(sub 1) to BN including the normal ***resistance*** ***elements*** R(sub 1) to RL. The distances between the blocks 10 and B(sub 1) and also between the blocks 11 and BN are set at the value equal to the mutual distances among the blocks B(sub 1) to BN Then both blocks 10 and 11 have the same shapes as those of blocks B(sub 1) to BN.

27/3,AB/13 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO
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05688687
TRANSMISSION BELT

PUB. NO.: 09-303487 [JP 9303487 A]
PUBLISHED: November 25, 1997 (19971125)
INVENTOR(s): TACHIBANA HIROYUKI
YAMAGUCHI KATSUYA
APPLICANT(s): BANDO CHEM IND LTD [000506] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 08-118650 [JP 96118650]
FILED: May 14, 1996 (19960514)

ABSTRACT

PROBLEM TO BE SOLVED: To improve the permanent set resistance and crack resistance by forming the partial element of a belt with the mixed phase of

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the ACSM phase using alkylated chlorosulfonated polyethylene as the rubber component and the phase using polyethylene halide as the rubber component.

SOLUTION: Three upper layers 2 of rubber canvas, an adhesive rubber layer 4 arranged with high-strength, low-ductility core wires 3, a compressed rubber layer 5 which is an elastic body layer, and a lower layer 2 of the rubber canvas are vertically laminated to form a V-belt 1. The compressed rubber layer 5 which is a part of the laminated V-belt 1 is formed with the mixed phase of the ACSM phase using alkylated chlorosulfonated polyethylene as the rubber component and the phase using polyethylene halide as the rubber component, and single fibers 6 are mixed while being oriented in the width direction of the belt 1. The heat ***resistance*** of belt elements is improved, and the permanent set resistance and crack resistance can be consistently improved.

27/3,AB/14 (Item 10 from file: 347)
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05646260
A/D CONVERTER

PUB. NO.: 09-261060 [JP 9261060 A]
PUBLISHED: October 03, 1997 (19971003)
INVENTOR(s): KUMAMOTO TOSHIO
MATSUMOTO OSAMU
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-072042 [JP 9672042]
FILED: March 27, 1996 (19960327)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce an area on a semiconductor chip required to arrange the converter.

SOLUTION: A ladder resistor 1 in which resistive elements r1, r2, ..., r8 are connected in series via taps T1, T2, ..., T7 is looped back at its midpoint. Couples of differential comparators such as differential comparators C1, C7 and differential comparators C2, C6 connected to common taps are arranged side by side so as to be close to be tap to be connected. Thus, the length of wiring to connect the taps T1, T2, ..., T7 and the differential comparators C1, C2, ..., C7 can be decreased, and then the area required for the wiring on a semiconductor chip can be reduced.

27/3,AB/15 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO
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05523360
KNOCKING DETECTOR

PUB. NO.: 09-138160 [JP 9138160 A]
PUBLISHED: May 27, 1997 (19970527)
INVENTOR(s): OMURA SHINJI
KATO YASUNARI
YAMAGUCHI KIMIaki

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APPLICANT(s): DENSO CORP [000426] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 07-295753 [JP 95295753]
FILED: November 14, 1995 (19951114)

ABSTRACT

PROBLEM TO BE SOLVED: To enhance the reliability while reducing the labor required for assembling work.

SOLUTION: A vibration detector 20 comprises a piezoelectric element 21, silver electrodes 22, 23, 25, and a load ***resistor*** 24. The piezoelectric element 21 is polarized in the reverse direction to the thickness direction on the opposite sides in radial direction. The load resistor 24 is printed using resistive paste between the silver electrodes 22, 23 of different polarity provided on one end face of the piezoelectric element 21 and the signal voltage of piezoelectric element 21 is generated across the load resistor 24. When a wire harness and a pair of caulked terminal plates are brought into contact with the silver electrodes 22, 23, respectively, signal voltage generated from the piezoelectric element 21 can be delivered to an ECU(electronic control unit). Since the terminal plate is required to be connected electrically with only one end face of the piezoelectric element 21, assembling work is facilitated. Furthermore, labor required for the assembling work can be reduced because the vibration detector 20 comprising arranged with the load resistor 24 can be handled as one component.

27/3,AB/16 (Item 12 from file: 347)
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05412305

METHOD FOR CONNECTING MAGNETIC HEAD

PUB. NO.: 09-027105 [JP 9027105 A]
PUBLISHED: January 28, 1997 (19970128)
INVENTOR(s): YAMAGUCHI KENICHI
APPLICANT(s): KAO CORP [000091] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 07-194135 [JP 95194135]
FILED: July 07, 1995 (19950707)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent the electrical damage of a magneto-resistive element by soldering the connecting part of the magneto-resistive element and a head driving circuit by using a non-electric soldering iron.

SOLUTION: A soldering device 20 fixes the coil element 13 of the magnetic head 11, the conductor 17 of the magneto-resistive element 14 and the terminal 19 disposed at the flexible printed circuit board, etc., on a head driving circuit 15 side to a working table 21 for soldering by fixing the magnetic head 11 thereto by means of lock screws 22 and placing the terminal 19 on a holding jig 23. Next, the conductor 17 is guided and positioned onto the terminal 19 and the required amount of cream solder is supplied to the connecting part of the conductor 17 and the terminal 19 by operating a cream solder supplying syringe 25, by which the connecting part is soldered by using a gas soldering iron 26. The magneto- ***resistive***

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element 14 is kept free from the electrical influence by using the non-electric soldering iron in such a manner, by which the electrical damage of the element 14 is prevented. The exertion of the damage by heating on the element 14 is averted as well by using the cream solder.

27/3,AB/17 (Item 13 from file: 347)
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04806881
RECEIVER OF INFRARED RAY SIGNAL

PUB. NO.: 07-099481 [JP 7099481 A]
PUBLISHED: April 11, 1995 (19950411)
INVENTOR(s): MIYAGAKI MASAHIITO
IGARASHI MICHIAKI
APPLICANT(s): SAKAI JUKOGYO KK [399503] (A Japanese Company or Corporation)
, JP (Japan)
APPL. NO.: 06-006502 [JP 946502]
FILED: January 25, 1994 (19940125)

ABSTRACT

PURPOSE: To use an indoor infrared ray receiving module for a receiver for an outdoor remote controller and to provide a receiver capable of receiving an infrared ray signal sent in every horizontal direction and in a upper or lower direction.

CONSTITUTION: A voltage is applied to a noninverting input terminal of a 1st stage operational amplifier 19, an output terminal of a photo diode is connected to an inverting input terminal, and the output terminal and the inverting input terminal off the 1st stage operational amplifier 19 are connected via a **resistive element**, the output terminal of the 1st stage operational amplifier 19 is connected to a noninverting input terminal of a 2nd stage operational amplifier 20 and an inverting input terminal and an output terminal of the 2nd stage operational amplifier 20 are connected and the output terminal is connected to the inverting input terminal of the 1st stage operational amplifier 19 via a **resistive element** and the output terminal of the operational amplifier 19 is connected to a general-purpose infrared ray receiving module 2.

27/3,AB/18 (Item 14 from file: 347)
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04260335
DIFFERENTIAL AMPLIFIER, COMPARATOR AND A/D CONVERTER

PUB. NO.: 05-252035 [JP 5252035 A]
PUBLISHED: September 28, 1993 (19930928)
INVENTOR(s): MIKI TAKAHIRO
KUMAMOTO TOSHIO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-048775 [JP 9248775]
FILED: March 05, 1992 (19920305)
JOURNAL: Section: E, Section Number 1487, Volume 18, Number 10, Pg. 60,

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January 10, 1994 (19940110)

ABSTRACT

PURPOSE: To prevent a delay of a time required for conversion and to obtain the A/D converter with a high operating speed by giving a converted analog input voltage directly to a comparator, that is, a differential amplifier circuit not through a ***resistive*** ***element*** or other ***element***.

CONSTITUTION: A signal sampled by a sample-and-hold circuit 11 is inputted to an A/D converter circuit 12 and a differential amplifier 14. The circuit 12 obtains conversion data $D(\text{sub } m+1)\text{-DK}$, of high-order bits and gives them to a D/A converter circuit 13, in which the data are converted into an analog signal. The differential amplifier 14 receives a signal sampled by the circuit 11 and an analog signal with the high-order bit restored thereto and outputs complementary or differential voltages $VA(\text{sub } 1)$, $VA(\text{sub } 2)$. Then the voltages $VA(\text{sub } 1)$, $VA(\text{sub } 2)$ are fed to an A/D converter circuit 15 as complementary or differential input signals and the A/D converter circuit 15 converts the voltages into low-order bit conversion data $D(\text{sub } 1)\text{-}D(\text{sub } m)$ and they are outputted. Since the converted analog input voltage is not directly given to the differential amplifier 14 in this way, the time delay in the conversion is prevented.

27/3,AB/19 (Item 15 from file: 347)
DIALOG(R)File 347:JAPIO
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03806657
SEMICONDUCTOR DEVICE AND D/A CONVERTER

PUB. NO.: 04-171757 [JP 4171757 A]
PUBLISHED: June 18, 1992 (19920618)
INVENTOR(s): KUMAMOTO TOSHIO
NAKAMURA YASUYUKI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-298687 [JP 90298687]
FILED: November 02, 1990 (19901102)
JOURNAL: Section: E, Section Number 1274, Volume 16, Number 478, Pg. 3, October 05, 1992 (19921005)

ABSTRACT

PURPOSE: To exhibit an excellent constant current characteristic by a construction wherein an electric **resistance** being a heating **element** is provided in the substrate of an MOS transistor and electrified from outside.

CONSTITUTION: An electric resistance R being a heating element is provided in an oxide film B of poor heat conduction of a substrate whereon an MOS transistor is formed, and it is electrified through a through hole T. Due to a heat generated by a current of the transistor, the inferior heat conduction of the oxide film B of the layer below the transistor and further the heat in the electric **resistance**, the **shift** of a channel in the transistor is reduced and a region wherein the saturation characteristic of the MOS transistor is not dependent on a drain-source voltage is produced. Thereby an excellent constant current characteristic is exhibited by a low gate voltage.

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27/3,AB/20 (Item 16 from file: 347)
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03403259
LAMINATE-TYPE SEMICONDUCTOR DEVICE

PUB. NO.: 03-066159 [JP 3066159 A]
PUBLISHED: March 20, 1991 (19910320)
INVENTOR(s): KONO HIROYUKI
KUMAMOTO TOSHIO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-203157 [JP 89203157]
FILED: August 04, 1989 (19890804)
JOURNAL: Section: E, Section Number 1076, Volume 15, Number 229, Pg. 47, June 11, 1991 (19910611)

ABSTRACT

PURPOSE: To obtain a laminate structure such as an inverter which can be integrated highly by a method wherein the inverter is formed in a first single-crystal layer and a means to adjust a threshold voltage of the inverter is formed in a second single-crystal layer under it.

CONSTITUTION: A back gate potential is impressed via an interlayer interconnection layer 4 formed under a p-type SOI layer 60 and via a **resistance element** 3 formed so as to be connected to the interlayer interconnection layer. A back gate voltage input terminal 15 is formed at the *****resistance***** *****element***** 3. A seed which transforms a polycrystalline layer into a single crystal may be used as the interlayer interconnection layer 4. A layer in which a CMOS inverter is formed and the **resistance element** 3 used to adjust a threshold voltage of the CMOS inverter are formed in different layers. Consequently, the CMOS inverter and the **resistance element** for back gate voltage adjustment use are not formed on the same plane as compared with conventional cases. As a result, the CMOS inverter can be integrated highly.

27/3,AB/21 (Item 17 from file: 347)
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03373151
THERMAL HEAD

PUB. NO.: 03-036051 [JP 3036051 A]
PUBLISHED: February 15, 1991 (19910215)
INVENTOR(s): YAMAGUCHI KIYOTAKA
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-172377 [JP 89172377]
FILED: July 03, 1989 (19890703)
JOURNAL: Section: M, Section Number 1108, Volume 15, Number 171, Pg. 52, April 30, 1991 (19910430)

ABSTRACT

PURPOSE: To detect burning of a thermal head automatically by a method wherein a resistor is inserted in parallel to a drive transistor of the thermal head, and a voltage value to be generated in the resistor is read.

CONSTITUTION: In the case of no burning in an heating element 2, when voltage is impressed to be the heating element 2, a current flows through the heating element 2 and a resistor 4, and a voltage value divided by each resistance value is outputted as output from the resistor 4. This voltage value is taken as high electric potential. When a drive transistor 3 is turned on, current hardly flows through the resistor 4, and output of the resistor becomes a value akin to ground voltage. This is taken as low electric potential. Then, in the case of burning in the heating element 2, output of the resistor 4 is at low electric potential as it is irrespective of being on or off of the drive transistor 3. Therefore, when voltage is impressed to the heating element 2 under a state in which the drive transistor 3 is off, high electric potential or low electric potential is outputted as output of the resistor 4 depending upon whether burning of the heating element 2 is present or not. A processor 5 reads output voltage of the resistor 4, and detects the presence of burning of the heating element 2.

27/3,AB/22 (Item 18 from file: 347)
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03226621

DIGITAL/ANALOG CONVERSION CIRCUIT

PUB. NO.: 02-202121 [JP 2202121 A]
PUBLISHED: August 10, 1990 (19900810)
INVENTOR(s): YAMAGUCHI KAZUhide
APPLICANT(s): NEC IC MICROCOMPUT SYST LTD [470861] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-021257 [JP 8921257]
FILED: January 30, 1989 (19890130)
JOURNAL: Section: E, Section Number 994, Volume 14, Number 489, Pg. 82, October 24, 1990 (19901024)

ABSTRACT

PURPOSE: To improve linear error characteristic by connecting a bias circuit to the intermediate point of the resistance element of a resistance string type digital/analog conversion circuit, and fixing a voltage at a desired contact voltage compulsorily.

CONSTITUTION: The resistance string type digital/analog conversion circuit 2 and the bias circuit 1 are connected between a reference voltage source 50 and a ground voltage, and the output of the bias circuit 1 is connected to the digital/analog conversion circuit 2. Since a very small resistance element compared with the resistance element 100 can be used as the resistance element 17 included in the bias circuit 1, the influence of a piezoelectric effect can be ignored, as well as an intermediate voltage can be generated with high accuracy. However, when it is desired to attain high accuracy with a level not being ignored in the offset voltage of a buffer amplifier 11, the higher accuracy can be attained by attaching a trimming circuit. In such a manner, the linear error characteristic can be improved.

27/3,AB/23 (Item 19 from file: 347)
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03074897
DATA HOLDING CIRCUIT

PUB. NO.: 02-050397 [JP 2050397 A]
PUBLISHED: February 20, 1990 (19900220)
INVENTOR(s): OGAWA KYOSUKE
SATO YASUSHI
KAWACHI MASA HARU
YAMAGUCHI KAZUYA
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
TOSHIBA MICRO ELECTRON KK [000000] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 63-200005 [JP 88200005]
FILED: August 12, 1988 (19880812)
JOURNAL: Section: P, Section Number 1045, Volume 14, Number 219, Pg. 131, May
09, 1990 (19900509)

ABSTRACT

PURPOSE: To decrease the through current value between a power source and a ground and to prevent the increase of the chip area of an integrated circuit by serially inserting **resistance elements** between the output of a CMOS type second inverting circuit, which feeds back the output of a CMOS type inverting circuit to its input, and the input of a first inverting circuit.

CONSTITUTION: A clocked inverter 15, which consists of two P channel MOS transistors (TR) 11 and 12 and N channel MOS TRs 13 and 14 respectively, an inverter 18, which consists of one P channel MOS TR 16 and N channel MOS TR 17 respectively, a clocked inverter 21, which consists of one P channel MOS TR 19 and N channel MOS TR 20 respectively, and a resistance 22 constitute the title circuit. Further, the resistance 22 is inserted between the output of the inverter 21 and the input of the inverter 18. Thus, the through current flowing between the power source and the ground can be decreased, and the chip size can be made smaller

27/3,AB/24 (Item 20 from file: 347)
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02462561
IMAGE SENSOR

PUB. NO.: 63-079461 [JP 63079461 A]
PUBLISHED: April 09, 1988 (19880409)
INVENTOR(s): **YAMAGUCHI KAZUFUMI**
MURATA TAKAHIKO
YAMAMOTO YASUNAGA
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company
or Corporation), JP (Japan)
APPL. NO.: 61-224470 [JP 86224470]

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09/960,495

FILED: September 22, 1986 (19860922)
JOURNAL: Section: E, Section Number 649, Volume 12, Number 314, Pg. 93, August
25, 1988 (19880825)

ABSTRACT

PURPOSE: To improve the linearity including an amplifier section by providing a nonlinearity of an opposite characteristic cancelling the nonlinearity of a photo transistor (TR) or a photoconductive element to a feedback ***resistor*** of a preamplifier of a sensor.

CONSTITUTION: A scanning circuit 3 generates an access pulse to drive photo-TR arrays 1, 2 sequentially in the charge storage mode, and one photoTR of the arrays 1, 2 is in the read state and an optical signal charge appears on a line 4 and a signal charge for noise cancel appears on a line 5 by the access pulse. The signal charge is stored in a parasitic capacitor of output terminals 4, 5 and amplified by input FET amplifiers 8-1, 8-2 and an operational amplifier 9. By giving the nonlinearity to a feedback circuit of the amplifier, the nonlinearity using the sensor itself is cancelled. The feedback circuit consists of a series circuit comprising a resistor 10, a diode 11 and a resistor 12

27/3,AB/25 (Item 21 from file: 347)
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01842820

VIBRATION AND SOUND WAVE DETECTOR USING PIEZOELECTRIC ELEMENT

PUB. NO.: 61-056920 [JP 61056920 A]

PUBLISHED: March 22, 1986 (19860322)

INVENTOR(s): YORINAGA MUNEO
YOKOIWA SUMIHARU
YAMAGUCHI KIMIYAKI

APPLICANT(s): NIPPON DENSO CO LTD [000426] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 59-178661 [JP 84178661]

FILED: August 28, 1984 (19840828)

JOURNAL: Section: P, Section Number 482, Volume 10, Number 220, Pg. 94, July
31, 1986 (19860731)

ABSTRACT

PURPOSE: To improve the reliability of mechanical strength, by arranging a resistor on the upper surface part of a piezoelectric element and on an upper electrode and side electrodes, polarizing the piezoelectric element, and bonding a conducting member to the side electrode on the outer surface and the lower side part of the piezoelectric element.

CONSTITUTION: On the surface of a piezoelectric element 1-1, an upper electrode 1-2, a lower electrode 1-3 and side electrode 1-4 are attached by using printing technology. Then a resistor 2 is arranged on both the electrode 1-2 and the electrodes 1-4 on the element 1-1 by using printing technology. Under this state, i.e., under the state a current does not flow through the ***resistor*** 2, the ***element*** 1-1 is polarized. Then the element 1-1 is bonded to a conducting member 1-5. Thus the detector is completed. In this way, deterioration of polarization characteristics due to burning and the burning of the resistor 2 due to the polarization voltage can be prevented.

27/3,AB/26 (Item 22 from file: 347)
DIALOG(R)File 347:JAPIO
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01805275

DETECTING CIRCUIT FOR THERMAL HEAD BURN-OUT

PUB. NO.: 61-019375 [JP 61019375 A]
PUBLISHED: January 28, 1986 (19860128)
INVENTOR(s): **YAMAGUCHI KIYOTAKA**
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 59-139935 [JP 84139935]
FILED: July 06, 1984 (19840706)
JOURNAL: Section: M, Section Number 488, Volume 10, Number 167, Pg. 132, June
13, 1986 (19860613)

ABSTRACT

PURPOSE: To enable burn-out or a deteriorated condition of the titled device to be judged before printing, by a construction wherein a detecting resistor connected in series with heating elements is provided, and a potential difference generated between both ends of the resistor is detected.

CONSTITUTION: The detecting resistor 6 connected in series with the heating elements 1, a potential difference detecting circuit 7, an A/D converter 8 and a microprocessor 9 for totally controlling printing are provided. When detecting burn-out, a printing-controlling circuit 4 cuts off a transformer 3, and a voltage of a power source 5 is impressed on the heating elements 1 through the detecting resistor 6. With an electric current passed to one of the elements 1 by driving a driver 2, a potential difference according to the **resistance** of the **element** 1 is generated between both ends of the resistor 6. The potential difference thus detected is converted into a digital quantity by the converter 8, and the quantity is read by the microprocessor 9. The microprocessor 9 compares the read value with preset digital values to judge the current condition to be a normal condition, a deteriorated condition or a burnt-out condition. The judgement is conducted for all of the heating elements, whereby it is possible to detect burn-out in the thermal head. In addition, scatter of *****resistances***** of the heating **elements** can be also detected on the basis of the read values.

27/3,AB/27 (Item 23 from file: 347)
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01577716

MAGNETIC ENCODER

PUB. NO.: 60-056216 [JP 60056216 A]
PUBLISHED: April 01, 1985 (19850401)
INVENTOR(s): **YAMAGUCHI KATSUMASA**
KAWADA KOICHI
SAKAGAITO YUKIO
MASAKI TAKESHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company)

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or Corporation), JP (Japan)
APPL. NO.: 58-165512 [JP 83165512]
FILED: September 08, 1983 (19830908)
JOURNAL: Section: P, Section Number 377, Volume 09, Number 186, Pg. 90, August
02, 1985 (19850802)

ABSTRACT

PURPOSE: To obtain a small and highly accurate magnetic encoder by arranging a flying head incorporating a magnetic **resistance** effect **element** facing a magnetic scale formed on a substrate and an inclination detector for detecting the inclination thereof.

CONSTITUTION: A flying head 6 incorporating a magnetic resistance effect element 7 levitates by a fixed value from the surface of a magnetic medium 3 on an air current following the rotation of a substrate 2. Under such a condition, an element 7 reads a magnetized pattern 4 written into the magnetic medium 3 to detect the revolutions and the angle of rotation of a rotating shaft 1. The direction of rotation thereof is detected with an inclination detector 12 provided on the flying head 6

27/3,AB/28 (Item 24 from file: 347)
DIALOG(R)File 347:JAPIO
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01499120

CHANNEL SELECTING DEVICE

PUB. NO.: 59-210720 [JP 59210720 A]
PUBLISHED: November 29, 1984 (19841129)
INVENTOR(s): **YAMAGUCHI KAZUYA**
KAWAHARA YASUhide
CHIKARA YOSHIHISA
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company
or Corporation), JP (Japan)
APPL. NO.: 59-074129 [JP 8474129]
FILED: April 13, 1984 (19840413)
JOURNAL: Section: E, Section Number 306, Volume 09, Number 75, Pg. 102, April
04, 1985 (19850404)

ABSTRACT

PURPOSE: To determine whether the reception is performed or not according to the combination of outputs of comparators by obtaining a tuning and a band switching voltage through a switching means, and inputting those voltages to comparators.

CONSTITUTION: When the reception of a 2CH is not performed, a channel selection voltage is supplied to negative and positive parts of the comparators 1 and 2 through *****resistance***** *****elements***** 13 and 14. Then, a variable **resistance element** 15 which absorbs the variance in a channel selection voltage is adjusted to hold the outputs of the comparators 1 and 2 both at 'L' and the output of an NOR circuit 7 at 'H'. When the negative electrode potential of a comparator 5 is set to a potential (i) in a figure by resistances 33 and 34 as the band switching voltage, its output is at 'L' and the output of a TR40 is at 'H', so that the output of an AND circuit 9 is at 'H'. Thus, an element 43 and a relay 44 are operated to open a switch 45, and consequently a supply power source Bv for a tuner is opened to inhibit the reception of the 2CH.

11/14/2003

09/960,495

27/3,AB/29 (Item 25 from file: 347)
DIALOG(R)File 347:JAPIO
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01390283

SUPERCONDUCTIVE INTEGRATED CIRCUIT RESISTANCE ELEMENT

PUB. NO.: 59-101883 [JP 59101883 A]
PUBLISHED: June 12, 1984 (19840612)
INVENTOR(s): **IGARASHI MASARU**
TAKEI KOJI
IWATA TSUNEKAZU
APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese
Company or Corporation), JP (Japan)
APPL. NO.: 57-211341 [JP 82211341]
FILED: December 03, 1982 (19821203)
JOURNAL: Section: E, Section Number 270, Volume 08, Number 217, Pg. 106,
October 04, 1984 (19841004)

ABSTRACT

PURPOSE: To obtain the titled element which has no fluctuation in electric resistance values due to the grain boundary scattering at an extremely low temperature and enables to increase the density of an integrated circuit by composing a **resistance element** of an amorphous thin film which contains Pd as the main constituent and contains a specific amount of Si.

CONSTITUTION: The **resistance element** is composed of the amorphous thin film which contain Pd as the main constituent and contains 15-23 atom % of Si. Or, it can be also composed of the one wherein a part of the main constituent Pd is replaced by Ag up to the maximum 0.25 at the atomic ratio to Pd, replaced by Cu up to the maximum 0.2 at the atomic ratio to Pd, or replaced by Au up to the maximum 0.25 at the atomic ratio to Pd. Then, the Pd-Si alloy thin film is deposited on a water-cooled Si substrate by sputtering a Pd-Si alloy target in Ar a plasma by using e.g. a usual RF sputtering device.

27/3,AB/30 (Item 26 from file: 347)
DIALOG(R)File 347:JAPIO
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01282425

PROTECTING CIRCUIT OF INPUT

PUB. NO.: 58-219825 [JP 58219825 A]
PUBLISHED: December 21, 1983 (19831221)
INVENTOR(s): **YAMAGUCHI KAZUO**
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 57-101602 [JP 82101602]
FILED: June 14, 1982 (19820614)
JOURNAL: Section: E, Section Number 235, Volume 08, Number 70, Pg. 105, April
03, 1984 (19840403)

ABSTRACT

PURPOSE: To obtain a protecting circuit having a high-voltage protecting **element resistive** to surge voltage having both positive and

negative polarity, by using a series circuit consisting of a diffused resistor arranged on the side of a signal input terminal as a protective resistor and a polycrystalline silicon resistor.

CONSTITUTION: The series circuit consisting of a diffused resistor 21 and a resistor 23 formed by a polycrystalline silicon layer is connected between a signal input terminal 1 and the initial stage MOSFET4 of an input circuit part so that the diffused resistor 21 is arranged on the input terminal 1 side. If p type silicon is used as a substrate for the diffused resistor 21, a diode 22 having the shown polarity is generated between the diffused resistor 21 and the substrate sub. The diode 22 is broken down by surge voltage generated when an MOSFET3, functioning as a positive overvoltage protecting element is turned on, divides the surge current to the substrate and turned to the forward direction with respect to the negative overvoltage input, so that the negative overvoltage is allowed to flow into the substrate to protect the FET4

27/3,AB/31 (Item 27 from file: 347)
DIALOG(R)File 347:JAPIO
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00719127

KNOCKING DETECTOR FOR INTERNAL COMBUSTION ENGINE

PUB. NO.: 56-039427 [JP 56039427 A]
PUBLISHED: April 15, 1981 (19810415)
INVENTOR(s): YAMAGUCHI KIMIYAKI
HATTORI TADASHI
OTSUKA YOSHINORI
APPLICANT(s): NIPPON SOKEN INC [414575] (A Japanese Company or Corporation)
, JP (Japan)
APPL. NO.: 54-115469 [JP 79115469]
FILED: September 07, 1979 (19790907)
JOURNAL: Section: P, Section Number 67, Volume 05, Number 96, Pg. 12, June 23,
1981 (19810623)

ABSTRACT

PURPOSE: To enhance the sensitivity of a detector to a significant extent by composing the detector of the magnetic vibrator which vibrates in response to the vibration of the engine and magnetization/magnetism sensing means, and making the resonance frequency of the detector meet knocking higher harmonic.

CONSTITUTION: The detector 2 is installed on a cylinder block with a threaded part 24a. The knocking vibration generated on the cylinder block is transmitted to the magnetic vibrator 21. Only one end of the magnetic vibrator 21 is fixed. Because of its size and shape such as designed to resonate to knocking vibration, the magnetic vibrator 21 significantly vibrates by the knocking vibration, changing the space distribution of a magnetic flux by magnet 22. This magnetic flux distribution change alters the resistance value of magnetic ***resistance*** **element*** 23. This resistance value change is amplified as a voltage change and a vibration by knocking is detected as a voltage vibration. Under this constitution, the resonance frequency of magnetic vibrator 21 is adjusted to meet the knocking higher harmonic, so that it is possible to enhance the sensitivity of a detector to a significant extent.

27/3,AB/32 (Item 28 from file: 347)
DIALOG(R)File 347:JAPIO
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00642617
CRYSTAL OSCILLATOR

PUB. NO.: 55-130217 [JP 55130217 A]
PUBLISHED: October 08, 1980 (19801008)
INVENTOR(s): CHIBA TADATAKA
YAMAGUCHI KAZUYOSHI
APPLICANT(s): KINSEKISHIYA KENKYUSHO KK [350836] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 54-037810 [JP 7937810]
FILED: March 29, 1979 (19790329)
JOURNAL: Section: E, Section Number 39, Volume 04, Number 189, Pg. 75,
December 25, 1980 (19801225)

ABSTRACT

PURPOSE: To eliminate substantially the frequency fluctuation due to the thermal stress for the crystal oscillator in which the heating electrode is provided on the crystal plate to secure the temperature compensation, by securing the overall neutralization for the internal distortion of the thermal stress inside the crystal plate which is caused by the heating electrode.

CONSTITUTION: Crystal plate 1' features the AT cut of 35 deg.14'. For the crystal oscillator, heating electrodes 6' and 7' are provided in the range of the right-left symmetric angle $\theta=120$ deg. of axis X to the center axis on the X-Z plane and axis X(sub 2) is tilted by angle α clockwise or counterclockwise centering on axis Y, and exciting electrodes 2' and 3' are provided on both surfaces respectively. In addition, electrodes 4' and 5' extended up to the circumference area are provided. The temperature control circuit to be connected to the crystal oscillator features a simple constitution in that the constant voltage is applied between both the terminals of the serial circuit of heater H of the heating electrode, positive characteristic temperature-sensitive **resistance** *****element***** TH and *****resistance***** R each. And elevation angle α is set between 4 deg. and 40 deg. in order to minimize the frequency fluctuation.

27/3,AB/33 (Item 29 from file: 347)
DIALOG(R)File 347:JAPIO
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00602126
TEMPERATURE MEASURING UNIT

PUB. NO.: 55-089726 [JP 55089726 A]
PUBLISHED: July 07, 1980 (19800707)
INVENTOR(s): KOBANE SUMIO
YAMAGUCHI KOSAKU
TAGUCHI KOJI
APPLICANT(s): MEISEI ELECTRIC CO LTD [351295] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 55-002747 [JP 802747]

11/14/2003

09/960,495

FILED: January 14, 1980 (19800114)
JOURNAL: Section: P, Section Number 29, Volume 04, Number 138, Pg. 125,
September 27, 1980 (19800927)

ABSTRACT

PURPOSE: To enable to perform accurate temperature measurement, by avoiding the pulse width from being affected from external conditions, in the temperature measurement using the circuit in which the **resistance** value of **element** converting the temperature into resistance value is converted into pulse width.

CONSTITUTION: When the balance of the bridge circuit is unbalanced and the voltage V_i is outputted, it is DC-amplified 2 and inputted to the pulse width modulator 3 to change the pulse width $t(\text{sub } s)$ of pulse train from the pulse generator 4. The pulse train receiving the pulse width modulation is inputted to the transistor 5 to control ON.OFF operation of the transistor 5 and the effective resistance value R_t between a-b. When the input voltage of the modulator 3 is decreased (increased), the pulse width $t(\text{sub } s)$ increases (decreases), and the effective resistance value R_t is decreased (increased). Thus, the bridge circuit keeps balancing and variable output is obtained so that the pulse width $t(\text{sub } s)$ can be determined with the value of the temperature conversion resistance R_l . By counting the pulse output through the gate control with the pulse of pulse width $t(\text{sub } s)$, the temperature sensed with the conversion resistor can be grasped

27/3,AB/34 (Item 30 from file: 347)
DIALOG(R)File 347:JAPIO
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00558909

METHOD OF MANUFACTURING SOLAR BATTERY

PUB. NO.: 55-046509 [JP 55046509 A]
PUBLISHED: April 01, 1980 (19800401)
INVENTOR(s): YAMAGUCHI KAZUFUMI
NAKAYAMA NOBUO
MATSUMOTO HITOSHI
IKEGAMI SEIJI
APPLICANT(s): AGENCY OF IND SCIENCE & TECHNOL [000114] (A Japanese
Government or Municipal Agency), JP (Japan)
APPL. NO.: 53-118668 [JP 78118668]
FILED: September 28, 1978 (19780928)
JOURNAL: Section: E, Section Number 14, Volume 04, Number 79, Pg. 65, June 07,
1980 (19800607)

ABSTRACT

PURPOSE: To manufacture an **element** of low surface **resistance**, by performing the gas-phase growth of an n-type CdS containing indium as an impurity on a p-type CdTe substrate maintained in a prescribed range of temperature and by setting the resistivity of the CdS at a prescribed value.

CONSTITUTION: A crucible 4 containing a CdS crystal 3 as an evaporated CdS source, another crucible 6 containing metallic indium 5 and the p-type CdTe substrate 8 fitted on a holder 7 are set in the core the tube 2 of an electric furnace 1 so that the crystal 3 is maintained in a temperature

range from 800-1110 deg.C, and metallic indium 5 is maintained in a temperature range from 300-800 deg.C and the substrate 8 is maintained in a temperature range from 350-550 deg.C. A gas feed pipe 9 and a gas exhaust pipe 10 are connected to the core tube 2 to fill a reducing gas in the core tube 2. These conditions are kept for a prescribed time so that the CdS and the indium are evaporated, an n-type CdTe layer 15 and an n-type CdS layer 14 are produced on the surface of the substrate 8 and the surface resistance of these layers is set at 10-100 ω /square. This results in raising the electromotive force of the element when it is used as a solar battery

27/3,AB/35 (Item 31 from file: 347)
DIALOG(R)File 347:JAPIO
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00515318

DEVICE TO DETECT NEGATIVE-RESISTANCE WAVEFORM OF SEMICONDUCTOR
ELEMENT

PUB. NO.: 55-002918 [JP 55002918 A]
PUBLISHED: January 10, 1980 (19800110)
INVENTOR(s): YAMAGUCHI KAZUO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 53-075374 [JP 7875374]
FILED: June 23, 1978 (19780623)
JOURNAL: Section: P, Section Number 1, Volume 04, Number 27, Pg. 150, March
07, 1980 (19800307).

ABSTRACT

PURPOSE: To check whether or not a semiconductor element is defective having negative resistance characteristics by extracting a part of a waveform that could be sampling without sampling a part of a waveform containing high-frequency components.

CONSTITUTION: Voltage V and current I of transistor 3 to be checked, which is impressed with a bias by sweep source 1, are detected and they are sampled by sample hold circuits 12a and 12b via amplifiers 5 and 6. Further, they are converted into digital data by A/D converters 13a and 13b. A/D converted values are input to memory 15 and stored as the characteristic waveform of the transistor. By memory read circuit 15, they are read out for each coordinate showing each voltage value. Discriminator 17 counts the number of coordinates having two or more values '0' or '1' and determines whether or not the number of such coordinates exceeds the preset reference number.

27/3,AB/36 (Item 32 from file: 347)
DIALOG(R)File 347:JAPIO
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00401292

VOLTAGE NON-LINEAR RESISTANCE ELEMENT

PUB. NO.: 54-053292 [JP 54053292 A]
PUBLISHED: April 26, 1979 (19790426)
INVENTOR(s): HONDA TETSUYA

11/14/2003

09/960,495

NAGASHIMA MASAHIKO
YAGI KIYOSHI
SHIBATA SEIJI
YAMAGUCHI KAZUO

APPLICANT(s): OTOWA DENKI KOGYO KK [365132] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 52-120233 [JP 77120233]
FILED: October 05, 1977 (19771005)

27/3,AB/37 (Item 33 from file: 347)
DIALOG(R)File 347:JAPIO
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00382096
VOLTAGE NONLINEAR **RESISTOR ELEMENT**

PUB. NO.: 54-034096 [JP 54034096 A]
PUBLISHED: March 13, 1979 (19790313)
INVENTOR(s): HONDA TETSUYA
NAGASHIMA MASAHIKO
YAGI KIYOSHI
SHIBATA SEIJI
YAMAGUCHI KAZUO

APPLICANT(s): OTOWA DENKI KOGYO KK [365132] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 52-099972 [JP 7799972]
FILED: August 19, 1977 (19770819)

27/3,AB/38 (Item 34 from file: 347)
DIALOG(R)File 347:JAPIO
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00178269
SEMICONDUCTOR DEVICE

PUB. NO.: 52-137269 [JP 52137269 A]
PUBLISHED: November 16, 1977 (19771116)
INVENTOR(s): KONDO RYUJI
YAMAGUCHI KEN
TORIYABE TATSU
OGIWARA TAKAAKI

APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 51-053274 [JP 7653274]
FILED: May 12, 1976 (19760512)
JOURNAL: Section: E, Section Number 11, Volume 02, Number 19, Pg. 11168, February 08, 1978 (19780208)

ABSTRACT

PURPOSE: To improve the reproducibility of a high-voltage-resistant MOS type semiconductor **element** wherein the concentration of impurities on the surface of the semiconductor substrate ranges from $10(\text{sup } 18)$ - $10(\text{sup } 20)$ $\text{cm}(\text{sup } -3)$ by specifying the concentration of synthetic impurities in the drain zone in such a way that the depth of the concentration in the former is made deeper than that in the latter.

11/14/2003

09/960,495

27/3,AB/39 (Item 35 from file: 347)
DIALOG(R)File 347:JAPIO
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00101985

VOLTAGE-NON-LINEAR-RESISTIVE ELEMENT

PUB. NO.: 52-060985 [JP 52060985 A]
PUBLISHED: May 19, 1977 (19770519)
INVENTOR(s): HONDA TETSUYA
YAGI KIYOSHI
SHIBATA SEIJI
YAMAGUCHI KAZUO
APPLICANT(s): OTOWA DENKI KOGYO KK [365132] (A Japanese Company or
Corporation), JP (Japan)
APPL. NO.: 50-137520 [JP 75137520]
FILED: November 14, 1975 (19751114)

27/3,AB/40 (Item 1 from file: 371)
000879324

Title: Amplificateur differentiel, comparateur et convertisseur
analogique/numerique rapide utilisant cet amplificateur.
Patent Applicant/Assignee: MITSUBISHI DENKI KK
Applicant Address: MITSUBISHI DENKI KABUSHIKI KAISHA- Deposant - 2-3
MARUNOUCHI 2-CHOME, CHIYODA-KU, TOKYO JAPON (JP)
Inventor(s): MIKI TAKAHIRO - C-O MITSUBISHI DENKI KABUSHIKI KAISHA LSI
KENKYUSHO, 1 MIZUHARA 4-CHOME, ITAMI-SHI, HYOGO-KEN JAPON (JP);
KUMAMOTO TOSHIO - C-O MITSUBISHI DENKI KABUSHIKI KAISHA LSI
KENKYUSHO, 1 MIZUHARA 4-CHOME, ITAMI-SHI, HYOGO-KEN JAPON
Legal Representative: CABINET PLASSERAUD
Document Type: Patent / Brevet
Patent and Priority Information (Country, Number, Date):
Patent: FR 2689338 - 19931001
Application: FR 932595 - 19930305
Priority Application: JP 9248775 - 19920305

Abstract:

Un convertisseur analogique/numerique rapide (15) comprend un circuit amplificateur differentiel perfectionne. Chaque comparateur (61) qui est incorpore dans le convertisseur recoit directement une tension d'entree analogique complementaire ou differentielle a convertir. Chaque comparateur comprend un circuit amplificateur differentiel qui compare une difference de tension d'entree analogique et une difference de tension de reference. Un signal binaire qui represente le resultat de la comparaison est applique a un codeur (4) par l'intermediaire d'un circuit de conversion en binaire. Une tension d'entree analogique qui ne doit pas etre convertie est directement appliquee au comparateur, c'est-a-dire au circuit amplificateur differentiel, sans passer par des composants ou des elements resistifs, ce qui evite un retard dans la conversion.

Legal Status (Type, Action Date, BOPI No, Description):
Publication 19931001 9339 Date published
Search Report 19950505 9518 Date Search Report published
Claim Mod Modified claim
Grant 19960105 9601 Date granted

EIC2800

Irina Speckhard

308-6559

11/14/2003

09/960,495

ETC2800

Irina Speckhard

308-6559

11/14/2003

09/960,495

(FILE 'HOME' ENTERED AT 10:24:57 ON 14 NOV 2003)

FILE 'STNGUIDE' ENTERED AT 10:25:11 ON 14 NOV 2003

FILE 'WPIX, INPADOC, JAPIO, PATOSEP, PATOSWO' ENTERED AT 10:25:28 ON 14
NOV 2003

L1 4 S JP2001-059948/AP,PRN

11/14/2003

09/960,495

L1 ANSWER 1 OF 4 WPIX COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2002-731511 [79] WPIX
DNN N2002-576672
TI Semiconductor device for analog circuit, has resistor elements formed on insulating oxide film and active regions in contiguous with resistor element.
DC U11 U13
IN AMISHIRO, H; IGARASHI, M; KUMAMOTO, T; YAMAGUCHI, K
PA (MITQ) MITSUBISHI ELECTRIC CORP; (MITQ) MITSUBISHI DENKI KK
CYC 2
PI US 2002123202 A1 20020905 (200279)* 19p
JP 2002261244 A 20020913 (200279) 13p
ADT US 2002123202 A1 US 2001-960495 20010924; JP 2002261244 A JP 2001-59948 20010305
PRAI JP 2001-59948 20010305
AB US2002123202 A UPAB: 20021209
NOVELTY - Several resistor elements (4) are formed using a MOS transistor gate layer on an insulating oxide film. Several active regions (3) are formed in contiguous with each resistor element cross-wire on both sides. The width of the oxide film is defined by an amount of shift in resistance value of the resistor elements.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for semiconductor device manufacturing method.
USE - Semiconductor device for analog circuit.
ADVANTAGE - Allows the oxide film to be divided into suitable strips, forestalling a concave formation at the center of the film upon polishing of the film by CMP, thereby enhancing dimensional accuracy of the resistor elements upon fabrication. By presetting width of the oxide film, it is possible for the resistor elements to constitute semiconductor devices whose reliability is high enough to meet high precision requirements.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of the semiconductor device.
Active regions 3
Resistor elements 4
Dwg.1A/14

L1 ANSWER 2 OF 4 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1

AN 185818053 INPADOC ED 20021022 EW 200242 UP 20030326 UW 200312
TI SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD.
IN AMISHIRO HIROYUKI; KUMAMOTO TOSHIO; IGARASHI MOTOSHIGE; YAMAGUCHI KENJI
INS AMISHIRO HIROYUKI; KUMAMOTO TOSHIO; IGARASHI MOTOSHIGE; YAMAGUCHI KENJI
PA MITSUBISHI ELECTRIC CORP
PAS MITSUBISHI ELECTRIC CORP
TL English
DT Patent
PIT JPA2 DOCUMENT LAID OPEN TO PUBLIC INSPECTION
PI JP 2002261244 A2 20020913
AI JP 2001-59948 A 20010305
PRAI JP 2001-59948 A 20010305

L1 ANSWER 3 OF 4 INPADOC COPYRIGHT 2003 EPO on STN

LEVEL 1

AN 184427783 INPADOC ED 20021002 EW 200239 UP 20021202 UW 200248
TI SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME.

IN AMISHIRO HIROYUKI; KUMAMOTO TOSHIO; IGARASHI MOTOSHIGE; YAMAGUCHI KENJI
INS AMISHIRO HIROYUKI; KUMAMOTO TOSHIO; IGARASHI MOTOSHIGE; YAMAGUCHI KENJI
INA JP; JP; JP; JP
PA MITSUBISHI DENKI KABUSHIKI KAISHA
PAS MITSUBISHI ELECTRIC CORP
PAA US

DT Patent

PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)

PI US 2002123202 AA 20020905

AI US 2001-960495 A 20010924

PRAI JP 2001-59948 A 20010305

OSCA 137:209422

AB A semiconductor device of the invention has a plurality of resistor elements formed on an element isolating oxide film in predetermined regions on a surface of a semiconductor substrate. Active regions are furnished close to the resistor elements. This allows the element isolating oxide film near the resistor elements to be divided into suitable strips, forestalling a concave formation at the center of the element isolating oxide film upon polishing of the film by CMP and thereby enhancing dimensional accuracy of the resistor elements upon fabrication.

L1 ANSWER 4 OF 4 JAPIO (C) 2003 JPO on STN

AN 2002-261244 JAPIO

TI SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

IN AMISHIRO HIROYUKI; KUMAMOTO TOSHIO; IGARASHI MOTOSHIGE; YAMAGUCHI KENJI

PA MITSUBISHI ELECTRIC CORP

PI JP 2002261244 A 20020913 Heisei

AI JP 2001-59948 (JP2001059948 Heisei) 20010305

PRAI JP 2001-5994820010305

SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002

AB PROBLEM TO BE SOLVED: To improve reliability, by forming resistance elements having desired shapes on an element isolating oxide film and enhancing the precision of a resistance value.

SOLUTION: In this semiconductor device, in which a plurality of the resistive elements 4 are formed on the element isolating oxide film 2 in a prescribed region formed on the surface of a semiconductor substrate 1, active regions 3 are arranged at positions adjacent to the resistance elements 4. Thereby the element isolating oxide film 2 in the vicinities of the resistance elements 4 can be partitioned in necessary regions, and the formation of a recessed part in a central part of the element isolation oxide film 2 can be restrained, when the film 2 is polished by a CMP method, so that the dimensional accuracy of the shapes of the resistive elements 4 can be improved.

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